Prom Programmer

Data I/O

The PROM Programmer People

DATA I/O
P.O. Box 1603, Bellevue, Washington 98009

Offices in: Anaheim Calif., San Jose Calif., Boston Mass., Chicago Illinois, Mûnchen, Germany.

Are you aware -

That Programmable Read-Only Memories are available from twelve major semiconductor manufacturers?

That over 30 combinations of configuration and type PROM's are commercially available and more are being developed each month?

That DATA I/O CORPORATION offers a complete line of fully automatic data handling programmers to program all manufacturers' PROMs of the four popular technologies (fusible link, Avalanche Induced Migration, MOS, MNOS)?

We believe that you are a part of that group of engineers that are interested in pushing the frontiers of solid state memory. Knowing your interest, we want to share with you a review of our present product line and find out if we may play a part in YOUR programmable memory future.

Specifications

Data I/O ROM Programmer I

Complete programmer, consists of integral 8 key keyboard; tape perforator (8 level, for one inch mylar or oil base tape); 8 level bi-directional tape reader; bit data display of tape, ROM, and buffer information; 0-999 digital word counter; auto-program and auto-verify modes, using ROM, tape, or buffer as data source; power interrupt indicator; device zero (or one) verify mode; interlocking controls. Ready for operation with device personality card(s), and socket module(s) specified.

105-125 VAC, 3A., 60 Hertz

Size: 24″ L × 19″ W × 8″ H

Shipping weight / size: 65 pounds, 37″ × 23″ × 14″.

Specifications for European model available on request.

Data I/O ROM Programmer II

Same as above, except without tape perforator and associated perforator electronics.

MSCR-1 Mark-Sense Card Reader Module

Complete with optical scanner reader module, line cord, instrument cables, interface electronics (as required depending on model and age of instrument) and 50 each I.B.M. type Mark-Sense cards. Ready for operation of automatically transferring pencil marked truth table cards to RAM memory for subsequent PROM programming.

Program Card (device personality)

Program cards available for most device types, including the manufacturing technologies of Avalanche Induced Migration (AIM), Fusible Link (FL), Metal Oxide Semi-conductor (MOS) and MNOS.

Device organizations which may be accommodated by the standard instruments, range from 32 x 8 to 512 x 8 and include all x4 configurations. Expanded memory and expanded address versions are available for new high density devices.

Options and Accessories

Plug in translator cards are offered for converting different tape codes to binary. These include ASCII/P-N, ASCII/H-L, ASCII/Hex and BCD—others on request.

Any commercially available socket types can be provided in single or dual configurations on the socket module.

Data Handling

Standard instrument provides

Data input source selection:

- ROM or RAM master devices(s)
- Integral 512 x 8 Bit buffer memory; expanded RAMS available
- Tape reader
- Keyboard entered data

Data output selection:

- PROM 1
- PROM 2
- PROM 1 + 2
- Integral buffer memory
- Tape perforator (Programmer I only)

General Construction

Unitized design allows all modes, options and accessories to incorporate in one attractive cabinet. Recessed cord wind completes the clean, compact appearance. All components are accessible for easy maintenance.

Circuitry is all solid state, plug-in PC board construction. Basic electronics are contained on 5 plug-in PC boards, plus 4 board power supply. All PC boards are of flow soldered construction.

Data I/O warrants the instrument to be free of defects in parts and workmanship for a period of one year.

Device Universality

The following technologies can be programmed:

- Avalanche Induced Migration (AIM) p/ROM's
- Fusible Link (FL) p/ROMs
- Metal Oxide Semiconductor (MOS) p/ROMs
- MNOS P-Channel technology

Simplicity:

The machine is similar in operation to secretarial equipment such as adding machines, typewriters, etc., and requires minimal operator training.

Reliability:

Serviceability and rugged modular design concepts have been strictly followed.

Production Sequencer:

As an aid to reliable, high-volume, production through-put, a plug-in module is available which causes the following automatic sequences:

- Continuity Test — to ensure proper device orientation and pin contacts
- Blank Test — which guarantees the device to be data-free
- Program — from selected data source
- Verify — compares programmed PROM with source data (and tests VOH and VOL levels where specified)

Each sequence is separately indicated.

"SEQUENCER" represents the world's first one button, *full* programming system.

THE FUTURE of programmable devices is highly dependent on The Programmer. Each IC manufacturer's product potential is enhanced by the advent of a truly *universal* programmer. The Data I/O ROM PROGRAMMERS promotes the future.

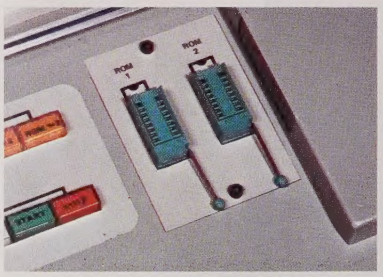
DATA I/O
P.O. Box 1603
Bellevue, Washington 98009
(206) 455-3990

Programmer I with Mark-Sense Card Reader (optional)

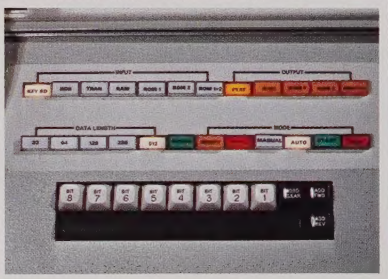
Programmer II

DATA I/O CORPORATION

PROM Programmer I and II

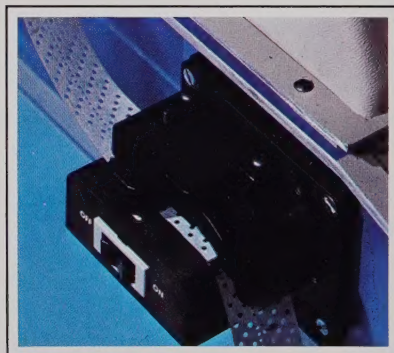


Socket Area Modular design allows complete flexibility. Socket module is dedicated to specific program card positions by simple plug configuration. Any commercially available socket type(s) may be provided. Capability to program multiple devices is available. High air volume fan, cools devices to allow faster program speeds.

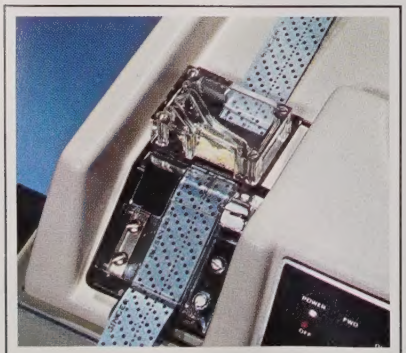


Keyboard/Mode Select Panel Keyboard entry allow production or modification of bit programs based on engineering notes, or truth table. Fast cycle forward and reverse function keys allow synchronous access to any word line in tape, buffer, or device.

Mode select section allows push-button access to a variety of input data sources, which may be programmed into or compared with any selected output; automatically or manually.



Tape Reader High speed tape reader, reads, programs, verifies in either forward or reverse directions. Automatically reverses direction at end of word count for performing auto-program or auto-verify operations without re-indexing. Synchronizes and reads in step with any output selected.

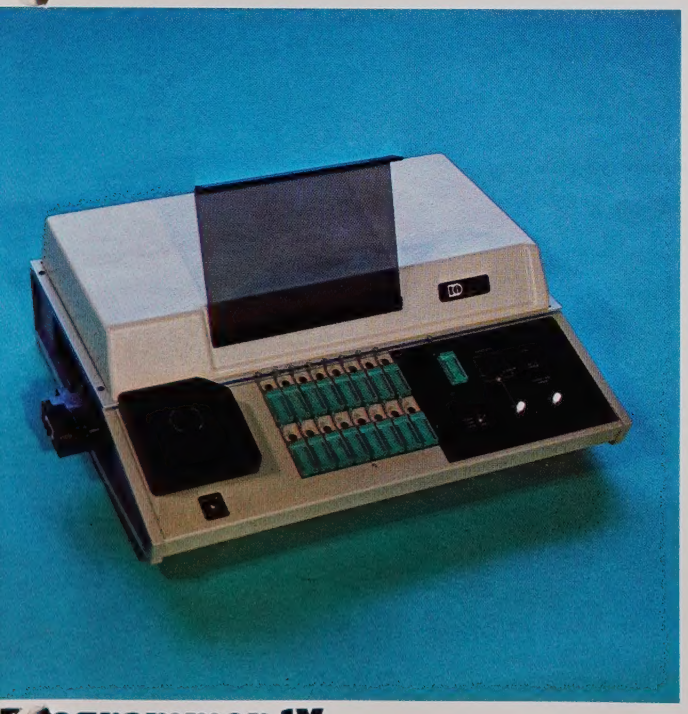


Paper Tape Perforator Integral heavy duty tape punch allows complete flexibility for inexpensive documentation of programs. Need for expensive master device stocking is eliminated. Modification and documentation of modified programs is readily accomplished.

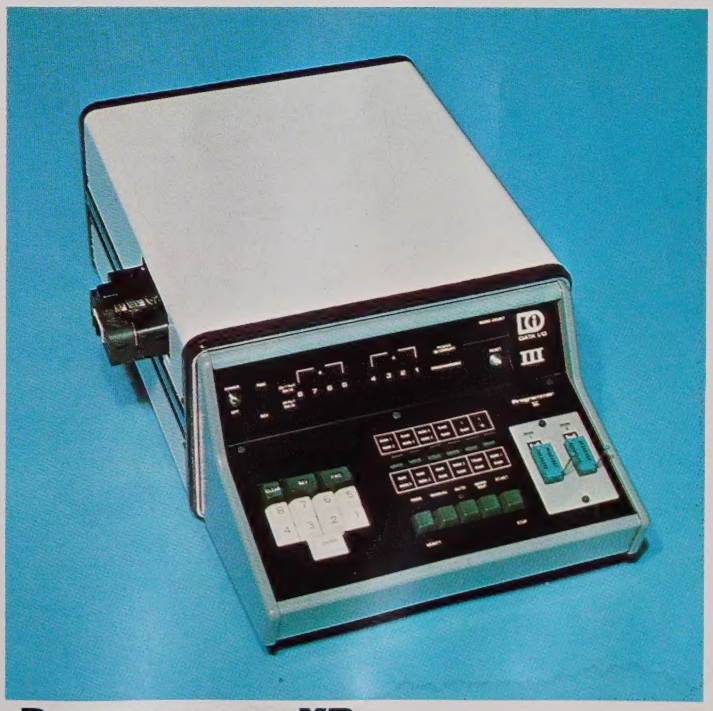
Display Panel The display panel allows visual observation of bit patterns from any data source and/or any output. Program pulse and position, power interrupt and forward/reverse indicators are logically arranged. Word count is displayed on easy to read, 5 × 7 dot matrix LED display.

Programmer I with Mark-Sense Card Reader (optional)

Programmer III R



Programmer IV



Programmer VB

(See Specs Back Page)

DATA I/O Programmer I

Complete Programmer, consisting of integral 8 key keyboard; tape perforator (8 level, for one inch mylar or oil base tape); 8 level tape reader; bit data display of tape, ROM, RAM and buffer information; 0-999 digital word counter; auto program and auto verify modes using ROM, paper tape, card reader or buffer memory data sources; power interrupt indicator; device zero (or one) verify mode; interlocking controls; card access cover, one standard socket module (specify). Ready for operation with optional device personality card(s) and read-only card(s) and other options selected.

105-125 VAC, 3A., 60 Hertz
(240 VAC, 50 Hertz version Available on request)
Size: 24L x 19W x 8H
Shipping Weight/Size: 65 pounds, 37 inches x 23 inches x 14 inches

DATA I/O Programmer III C (Computer)

Basic universal instrument consists of Main Electronic Unit (MEU); Programmable Power Supply providing voltages in the range of 1 to 50 volts at current limits from 0.05 to 5.0 amperes; socket module mount; panel for I/O bit position display; word count display; reverse/forward address direction control and indicators; forward/reverse address slew control; power on/off switch; provision for remote input device interface; I/O select switches; standard 16/24 pin socket module. Ready for operation with optional device personality card (s), read-only card(s), and other options selected.

105-125 VAC, 3A., 60 Hertz
Size: 22L x 13W x 8H inches
Shipping Weight/Size: 55 pounds, 38L x 23W x 14H inches

Programmer III R (Reader)

Same as above except with integral paper tape reader (5-8 level I-R) and data clear control.

DATA I/O Programmer IV

Complete Programmer, consisting of programmable micro-computer controller, power supply, control panel, socket panel comprised of 16 each, 24 pin positive locking programming sockets and one master ROM socket, display, mode select panel for selection and LED display of test and programming modes, LED indicators for display of specific ROM status, provisions for paper tape reader mounting. Entire system attractively packaged in low silhouette housing and ready for "gang" programming of up to 16 MOS p/ROMs of any manufacturer specified at time of order.

105-125 VAC, 3A., 60 Hertz
(240 VAC, 50 Hertz version Available on request)
Size: 24L x 19W x 8H
Shipping Weight/Size: 65 pounds, 37 inches x 23 inches x 14 inches

PAPER TAPE READER (accessory)
5 to 8 level, optical (I-R), complete with associated plug-in electronics, cables and mounting hardware.

DATA I/O Programmer VB (Binary)

Basic universal instrument consists of Main Electronics Unit (MEU); Programmable Power Supply providing voltages in the range of 1 to 50 volts at current limits from 0.05 to 5.0 amperes; socket module mount; panel for I/O bit position display; word count display; reverse/forward address direction control and indicators; forward/reverse address slew control; power on/off switch; provision for Mark-Sense Card Reader interface and other remote input or output devices; I/O select switches; standard 16/24 pin socket module; 512 x 8 bit RAM; integral paper tape reader (5 to 8 level, I-R); binary keyboard, including fast forward/reverse and data clear controls. Ready for operation with optional device personality card (s), read-only card (s), and other options selected.

105-125 VAC, 3A., 60 Hertz
Size: 22L x 13W x 8H inches
Shipping Weight/size: 55 pounds, 38L x 23W x 14H inches

DATA I/O Programmer V O (Octal)

Same as above except with octal keyboard, including data clear control: octal data read-out and digital address display.

DATA I/O Programmer V H (Hexidecimal)

Same as above except hexidecimal keyboard, including data clear control: hex data read-out and decimal address display.

TABLE OF CONTENTS

		Page
	INTRODUCTION	1
Section 1	OPERATING INSTRUCTIONS	
1.1	General	1-1
1.2	Preparing for Operation	1-1
1.3	Display Panel	1-1
1.3.1	Word Counter Display	1-1
1.3.2	Reset Switch	1-1
1.3.3	Power Interrupt Indicator	1-1
1.3.4	Forward and Reverse Indicators	1-1
1.3.5	Programming Indicator	1-1
1.3.6	Data A and Data B Indicators	1-1
1.3.7	Input Data Indicators	1-2
1.3.8	Output Data Indicators	1-2
1.4	Keyboard Switches	1-2
1.4.1	Bit 1 Through Bit 8	1-2
1.4.2	Word Clear	1-2
1.4.3	Entry Bar	1-2
1.4.4	Add Fwd Key	1-2
1.4.5	Add Rev Key	1-2
1.5	Control Switches	1-3
1.5.1	Input Section Switch	1-3
1.5.1.1	Keybd Switch	1-3
1.5.1.2	Rdr Switch	1-3
1.5.1.3	Tran Switch	1-3
1.5.1.4	Ram Switch	1-3
1.5.1.5	Rom 1 Switch	1-3
1.5.1.6	Rom 2 Switch	1-3
1.5.1.7	Rom 1+2 Switch	1-3
1.5.2	Output Section	1-3
1.5.2.1	Perf Switch	1-3
1.5.2.2	Ram Switch	1-4
1.5.2.3	Rom 1 Switch	1-4
1.5.2.4	Rom 2 Switch	1-4
1.5.2.5	Rom 1+2 Switch	1-4
1.6	Mode Switch Assembly	1-4
1.6.1	Data Length Section	1-4
1.6.1.1	32 Switch	1-4
1.6.1.2	64 Switch	1-4
1.6.1.3	128 Switch	1-4
1.6.1.4	256 Switch	1-4
1.6.1.5	512 Switch	1-4
1.6.2	Mode Section	1-5
1.6.2.1	Insert Switch	1-5
1.6.2.2	Verify Switch	1-5
1.6.2.3	Program Switch	1-5
1.6.2.4	Manual Switch	1-5
1.6.2.5	Auto Switch	1-5

TABLE OF CONTENTS (Continued)

		Page
Section 1	OPERATING INSTRUCTIONS (Continued)	
1.6.2.6	Start Switch	1-5
1.6.2.7	Stop Switch	1-5
1.7	Card Installation and Change	1-5
1.7.1	Addmaster Reader/Driver 2 or Addmaster Reader/Driver 3 (J1-M RDR)	1-6
1.7.2	Perf Driver Assembly (J2-M PERF) Programmer I Only	1-6
1.7.3	Program Card One (J3-M PROM 1)	1-6
1.7.4	Program Card Two (J4-M PROM 2)	1-6
1.7.5	Spare (J5-M SPARE)	1-6
1.7.6	Translator (J6-M TRANS) (Optional)	1-6
1.7.7	Ram Buffer Assembly (J7-M RAM)	1-6
1.7.8	Address Card Assembly (J8-M ADD)	1-6
1.7.9	Control Card Assembly (J9-M CONTROL)	1-6
1.8	Operating Instructions	1-6
1.8.1	Clear Ram	1-7
1.8.2	Keybd to Perf (Programmer I Only)	1-7
1.8.3	Keybd to Ram	1-8
1.8.4	Keybd to Rom	1-10
1.8.5	Reader to Perf	1-10
1.8.5.1	Without Indexing	1-10
1.8.5.2	With Indexing	1-11
1.8.6	Rdr to Ram	1-12
1.8.6.1	Without Indexing	1-12
1.8.6.2	With Indexing	1-13
1.8.7	Rdr to Rom	1-14
1.8.7.1	Without Indexing	1-14
1.8.7.2	With Indexing	1-15
1.8.8	Tran (Translator) to Perf (Optional)	1-16
1.8.8.1	Without Indexing Code	1-16
1.8.8.2	With Indexing Code	1-17
1.8.9	Tran (Translator) to Ram (Optional)	1-18
1.8.10	Ram to Perf (Programmer I Only)	1-19
1.8.10.1	Standard Operation	1-19
1.8.10.2	Insert Indexing	1-21
1.8.11	Ram to Rom	1-22
1.8.12	Rom to Perf (Programmer I Only)	1-23
1.8.12.1	Without Index Code	1-23
1.8.12.2	Insert Indexing	1-24
1.8.13	Rom to Ram	1-26
1.8.14	Rom to Rom	1-26
1.8.15	Mark Sense Card Reader to Ram (Optional)	1-27
1.8.16	Blank Checking (Verification of an Unprogrammed Prom)	1-28
Section 2	PROGRAM (PERSONALITY) CARD INSTALLATION	
2.1	General	2-1
2.2	Mos Program Cards	2-1
2.3	Fuseable Link Program Cards	2-1
2.4	Avalanche Induced Migration Program Cards	2-2

TABLE OF CONTENTS (Continued)

		Page
Section 3	FUNCTIONAL DESCRIPTION	
3.1	General	3-1
3.2	Power Supply Assembly (203-24125)	3-1
3.3	Modular Power Supply Meu Connector Assembly (201-24532)	3-1
3.4	Modular +5 Volt Power Supply (201-24528)	3-1
3.4.1	Oscillator	3-2
3.4.2	Reference Volt	3-2
3.4.3	Plus 5 Volt Supply	3-2
3.5	Modular +24 Volt Power Supply Assembly (201-24526)	3-2
3.5.1	Minus 9 and Minus 5 Volt Regulator	3-2
3.5.2	Plus 24 Volt Regulators	3-2
3.6	Modular Programmable Power Supply Assembly (201-23530)	3-2
3.6.1	Positive Regulator	3-2
3.6.2	Negative Regulator	3-3
3.7	AC Motor Controlled Assembly (201-24607)	3-3
3.8	Perforator	3-3
3.9	Tape Reader Assembly (104-25548)	3-5
3.10	Keyboard Switch Assembly (201-23799)	3-6
3.11	Control Switch Assembly (201-24129)	3-6
3.11.1	Input Section	3-6
3.11.1.1	Key (S1)	3-6
3.11.1.2	Rdr (S2)	3-6
3.11.1.3	Tran (S3)	3-6
3.11.1.4	Ram (S4)	3-6
3.11.1.5	Rom 1 (S5)	3-6
3.11.1.6	Rom 2 (S6)	3-7
3.11.1.7	Rom 1+2 (S7)	3-7
3.11.2	Output Section	3-7
3.11.2.1	Perf (S8)	3-7
3.11.2.2	Ram (S9)	3-7
3.11.2.3	Rom 1 (S10)	3-7
3.11.2.4	Rom 2 (S11)	3-7
3.11.2.5	Rom 1+2 (S12)	3-7
3.12	Mode Switch Assembly (201-24545)	3-7
3.12.1	Data Length Section	3-8
3.12.1.1	512 (S17)	3-8
3.12.1.2	256 (S16)	3-8
3.12.1.3	128 (S15)	3-8
3.12.1.4	64 (S14)	3-8
3.12.1.5	32 (S13)	3-8
3.12.2	Mode Section	3-8
3.12.2.1	Program (S20)	3-8
3.12.2.2	Verify (S19)	3-8
3.12.2.3	Insert (S18)	3-8
3.12.2.4	Auto (S22)	3-9
3.12.2.5	Manual (S21)	3-9
3.12.2.6	Start (S23)	3-9
3.12.2.7	Stop (S24)	3-9

TABLE OF CONTENTS (Continued)

		Page
Section 3	FUNCTIONAL DESCRIPTION (Continued)	
3.13	Display Panel (201-23749)	3-9
3.13.1	Indicators	3-9
3.13.2	Word Counter	3-10
3.13.3	Word Count Reset	3-10
3.14	MEU Connector Assembly (Prog. I 201-24093) (Prog. II 201-24927)	3-10
3.15	Reader Driver Assembly, Addmaster No. 2 (201-24569)	3-10
3.15.1	Reader Start	3-10
3.15.2	Reader Advance and Reset	3-11
3.16	Reader Driver Assembly, Addmaster No. 3 (201-26963)	3-11
3.16.1	Tape Reader Operation	3-11
3.16.1.1	Reader Start	3-11
3.16.1.2	Reader Advance and Reset	3-12
3.16.2	Mark Sense Card Reader Operation	3-13
3.16.2.1	Card Reader Disable	3-13
3.16.2.2	Card Reader Strobe	3-13
3.16.2.3	Mod 32 Counter	3-13
3.17	Control Card Assembly (201-24810)	3-14
3.17.1	Forward/Reverse	3-14
3.17.2	Data I/O Buffer	3-14
3.17.3	Verify	3-15
3.17.4	Master Clock and Strobe Function Decoder	3-15
3.17.5	Mode Control	3-16
3.17.5.1	Manual	3-16
3.17.5.2	Auto	3-17
3.17.5.3	Limit Memory	3-17
3.17.6	Power Interrupt	3-18
3.18	Address Card Assembly (201-24133)	3-18
3.18.1	Binary Counter	3-18
3.18.1.1	Count Up	3-18
3.18.1.2	Count Down	3-18
3.18.1.3	Reset	3-18
3.18.2	Binary to BCD Converter	3-18
3.18.2.1	Example 1 (33)	3-20
3.18.2.2	Example 2 (170)	3-20
3.18.2.3	Example 3 (341)	3-20
3.19	Ram Buffer (201-24137)	3-21
3.19.1	Addressing	3-21
3.19.2	Data Input	3-21
3.19.3	Write	3-21
3.19.4	Read	3-22
3.19.5	Read and Write	3-22
3.20	Perf Driver (201-24521)	3-22
3.20.1	Code Perforation	3-22
3.20.2	Turn-On Conditioner	3-23
3.20.3	6-Level/8-Level	3-23
3.20.4	Forward Feed, Reverse Feed and Perf Inhibit Inputs	3-23
3.21	Interface Assemblies (201-24214 and 201-24543)	3-23

TABLE OF CONTENTS (Continued)

		Page
Section 4	**CIRCUIT BOARD LAYOUT AND PARTS LIST**	
4.1	General	4-1
4.2	Rom Programmer System	4-1
4.2.1	Front View	4-1
4.2.2	Rear View	4-1
4.2.3	Bottom Inside View	4-2
4.2.4	Top Inside View	4-2
4.2.5	Power Supply Assembly (203-24125)	4-3
4.3	Rom Programmer Circuit Boards	4-4
4.3.1	MEU Power Supply Assembly (201-24532)	4-4
4.3.2	+5 Volt Power Supply Assembly (201-24528)	4-5
4.3.3	+24 Volt Power Supply Assembly (201-24526)	4-6
4.3.4	Programmable Power Supply Assembly (201-24530)	4-7
4.3.5	AC Motor Control Assembly (201-24607)	4-7
4.3.6	MEU Connector Assembly (201-24093/201-24927)	4-8
4.3.7	Assembly Front Panel (201-23749)	4-9
4.3.8	Control Switch Assembly (201-24129)	4-9
4.3.9	Mode Switch Assembly (201-24545)	4-10
4.3.10	Addmaster Reader/Driver 2 Assembly (201-24569)	4-11
4.3.11	Addmaster Reader/Driver 3 Assembly (201-26963)	4-12
4.3.12	Control Card Assembly (201-24810)	4-13
4.3.13	Address Card Assembly (201-24133)	4-14
4.3.14	Ram Buffer Assembly (201-24137)	4-15
4.3.15	Perf Driver Assembly (201-24521)	4-16
Section 5	**SYSTEM INSTALLATION AND CHECK-OUT PROCEDURE**	
5.1	General	5-1
5.2	Power	5-1
5.3	Functional Check-Out	5-1
5.3.1	Indicator Check	5-1
5.3.2	Verify Circuits	5-3
5.3.3	Tape to Ram Step 1	5-4
5.3.4	Tape to Ram Step 2	5-4
5.3.5	Tape to Ram Step 3	5-4
5.3.6	Ram to Perforator	5-5
5.3.7	Card Reader Check (Optional)	5-6
Section 6	**MAINTENANCE**	
6.1	Lubrication	6-1
6.1.1	Perforator (Programmer I Only)	6-1
6.1.2	Perforator Driver Motor (Programmer I Only)	6-1
6.1.3	Fan Motor	6-1
6.1.4	Rom Fan Motor	6-1
6.1.5	Paper Tape Reader	6-1
6.2	Preventative Maintenance	6-3
6.2.1	Check List	6-3
6.2.2	Machine Check Out	6-3
6.3	Regulated Power Supply Voltage and Adjustment	6-3
6.3.1	Regulated +5 Volts DC	6-3
6.3.2	Regulated -9 Volts DC	6-3

LIST OF TABLES

		Page
3.1	SN74185A Truth Table	3-19
5.1	Card Test Truth Table	5-7
6.1	Punch Preventative Maintenance Lubrication	6-2

LIST OF ILLUSTRATIONS

3.1	Punch Operation	3-4
3.2	Connector Board	3-5
6.1	Punch Lubrication	6-1

LIST OF SCHEMATICS

021-11460	Interconnect Diagram
018-11837	Rom Programmer Block Diagram
203-24125	Power Supply Assembly
201-24532	MEU Power Supply Assembly
201-24528	+5 Volt Power Supply Assembly
201-24526	+24 Volt Power Supply Assembly
201-24530	Programmable Power Supply Assembly
201-24607	AC Motor Control Assembly
212-23799	Keyboard Switch Assembly
201-24129	Control Switch Assembly
201-24545	Mode Switch Assembly
201-23749	Display Panel
201-24093	MEU Connector Assembly (Programmer I)
201-24927	MEU Connector Assembly (Programmer II)
201-24569	Addmaster Reader/Driver 2 Assembly
201-26963	Addmaster Reader/Driver 3 Assembly
201-24810	Control Card Assembly
018-11898	Control Card Timing Diagram (Sheets 1 and 2)
201-24133	Address Card Assembly
201-24137	Ram Buffer Assembly
201-24521	Perf Driver Assembly
201-24214	Interface Assembly, Dual 16 Pin
201-24543	Interface Assembly, Dual 24 Pin

INTRODUCTION

The Data I/O Programmers are designed as universal instruments to program all commercially available programmable Read-Only Memory devices.

The Programmer I and Programmer II are identical with the exception of the Paper Tape Perforator which is included as an integral part of the Programmer I. This Perforator and its associated electronic circuits allow the operator to punch an eight-level paper tape for a permanent record of any program that could be required for future use. Both Programmers have the capability of reading a tape punched by another machine.

Program characteristics for each PROM type may be obtained by simply installing the Program (Personality) Printed Circuit card or cards peculiar to the device to be programmed.

Offered as options to both models are an ASCII Translator and a Mark Sense Card Reader.

The ASCII Translator card allows the Programmer to read an ASCII coded tape and translate it into the binary coded data required by the Programmer. The data may be input from the Reader to the internal Random Access Memory (RAM) from which it is output to the programmable device or to the Perforator for a tape record.

The Mark Sense Card Reader provides a method for truth tables (programs) to be written in pencil on a card and read directly into the RAM from which it may be output to either a programmable device or a tape record.

All controls are located on a panel which provides convenient access. They are interlocked and designed for easy operator familiarization and use.

SECTION 1
OPERATING INSTRUCTIONS

1.1 GENERAL

The ROM Programmers Model I and II are designed to provide the capability of programming one or two Programmable Read Only Memories (PROM) from an assortment of Input devices. Both models contain a 512 x 8 programmable Random Access Memory (RAM) used as an intermediate storage device. It can be used as input and/or output. The Programmer I contains a Perforator with its associated circuitry to provide a permanent copy of any programs to be entered into a PROM.

1.2 PREPARING FOR OPERATION

Plug the power cord into a 3 wire 115 VAC or 220 VAC, as applicable, receptacle. Turn the system ON by moving the POWER switch on the Display Panel to the UP position. The "Power Interrupt" indicator should come ON. All other indicators will be random varying according to switch positions. The Cooling fan in the Baseplate assembly should operate.

1.3 DISPLAY PANEL

The Display Panel contains a number of single unit indicators plus three 7-segment display units. These indicators display the Programmer operation as described in the following sub-paragraphs.

1.3.1 Word Counter Display

The Word counter consists of three light emitting diode display lamps. It will show the address contained in the Word counter on the Address Card assembly.

1.3.2 Reset Switch

When the RESET switch is depressed it will apply a LOW to the Word counter and reset the counter to zero. The Counter display will reflect the address in the counter and will read zero. The Master Clock on the Control card will be initialized at the same time.

1.3.3 Power Interrupt Indicator

If power has been removed this indicator will come ON when power is restored. It is a visual indication to the operator that power has been removed and the contents of the RAM have been lost. The indicator will be extinguished when the START switch is depressed and stay OFF until the next time that power has been removed and restored.

1.3.4 Forward and Reverse Indicators

One indicator will be illuminated at a time to inform the operator whether the address will be incremented or decremented when the Word counter is stepped.

1.3.5 Programming Indicator

This indicator will be illuminated with PROG selected and a Write strobe to program data into the Output device.

1.3.6 Data A and Data B Indicators

These LED's will identify whether the four most significant (B) or four least

significant (A) bits or both are being programmed. If RAM is selected as the output both indicators will be illuminated. If one of the ROM switches has been selected the state of the indicators will be controlled by the two Program cards.

1.3.7 Input Data Indicators

These eight LED indicators give the status of the eight bits of input data from the selected Input device.

1.3.8 Output Data Indicators

These eight LED indicators give the status of the eight bits of output data from the selected Output device at the address shown on the Word Counter display.

1.4 KEYBOARD SWITCHES

All of the keyswitches on the keyboard are connected so that they will operate only if KEYBD is selected on the Input section and AUTO is **not** selected on the Mode section.

1.4.1 Bit 1 Through Bit 8

Enters data into the appropriate bit of the internal data register when that BIT switch is depressed.

1.4.2 Word Clear

Clears the data from the internal data register that has been entered from the BIT switches.

1.4.3 Entry Bar

Depressing the ENTRY BAR will cause the Word counter to either be incremented or decremented, depending on the direction selected, transferring at the same time the data in the selected Input device into the selected Output device.

Momentarily depressing and releasing the ENTRY BAR will cause the Word counter to change states by a count of one. If the key is held depressed in excess of approximately one quarter of a second the counter will start changing the count at a cyclic rate of 9 and 10 counts per second and will continue to do so until the keyswitch is released. Data will be transferred from the selected Input device to the selected Output device at each address, if PROG has been selected.

1.4.4 Add Fwd Key

Depressing this keyswitch will change the status of the counter to forward if it had been in reverse. At the same time the counter will increment one address. The ADD FWD keyswitch is a cyclic switch and will operate in the same manner as the ENTRY BAR,if it is not released within approximately one quarter second.

If the switch has not been released when the counter reaches the upper limit, the counter will hold.

1.4.5 Add Rev Key

This keyswitch operates in the same manner as the ADD FWD except the counter decrements. It will change the indicator to "REV" if it had been "FWD", it will count down one time or until released and will stop at the lower limit if not released.

1.5 CONTROL SWITCHES

The Control switches are divided into the Input and Output sections. All switches are self-illuminating when depressed.

1.5.1 Input Section Switch

The Input section consists of seven interlocked pushbutton switches. The KEYBD switch is free to operate in conjunction with any one other switch in the Input section. The other six switches are interlocked so that only one switch is depressed or closed at a time. Depressing one switch automatically opens the switch that had been closed.

1.5.1.1 Keybd Switch

Depressing this switch will enable the keyswitches on the keyboard provided the AUTO switch on the Mode Switch assembly is **not** closed.

1.5.1.2 Rdr Switch

Depressing this switch will enable the Tape Reader and Reader Driver circuitry.

1.5.1.3 Tran Switch

Depressing this switch will enable the optional ASCII Translator circuitry and the Tape Reader/Reader Driver.

1.5.1.4 Ram Switch

Depressing this switch will enable the Read circuits in the Random Access Memory (RAM).

1.5.1.5 Rom 1 Switch

Depressing this switch will enable the Input selection portion of any optional Program card or Read Only card installed in the J3-M connector on the MEU labeled PROM 1.

1.5.1.6 Rom 2 Switch

Depressing this switch will enable the Input selection portion of any optional Program card or Read Only card installed in the J4-M connector on the MEU labeled PROM 2.

1.5.1.7 Rom 1+2 Switch

Depressing this switch will enable the Input selection portion of any optional Program card or Read Only card installed in both J3-M and J4-M connectors on the MEU. Jumpers on the cards will have to be installed in the proper format to place the data from one into the four most significant bits and from the other into the four least significant bits.

1.5.2 Output Section

The five interlocked pushbutton switches in the Output section are ganged so that only one may be depressed at any time. Depressing another will automatically open any switch previously closed.

1.5.2.1 Perf Switch

Depressing this switch will apply AC voltage to the Perforator Driver motor provided PROG on the Mode Switch assembly has been selected.

1.5.2.2 Ram Switch

Depressing this switch will enable the Write circuits in the Random Access Memory (RAM).

1.5.2.3 Rom 1 Switch

Depressing this switch will enable the Output selection portion of any optional Program card or Read Only card installed in the J3-M connector on the MEU labeled PROM 1. AC power will be applied to the ROM Cooling fan at the same time.

1.5.2.4 Rom 2 Switch

Depressing this switch will enable the Output selection portion of any optional Program card or Read Only card installed in the J4-M connector on the MEU labeled PROM 2. AC power will be applied to the ROM Cooling fan at the same time.

1.5.2.5 Rom 1+2 Switch

Depressing this switch will enable the Output selection portion of both optional Program cards installed in J3-M and J4-M connectors on the MEU. Jumpers on the Program card will have to be placed to select which card will accept the four most significant bits and which of the four least significant bits. AC power will be applied to the ROM Cooling fan at the same time.

1.6 MODE SWITCH ASSEMBLY

The Mode switch bank is divided into two sections. One labeled Data Length and the other Mode. All switches are self-illuminating when depressed.

1.6.1 Data Length Section

The five switches in the Data Length section are interlocked so that only one switch can be depressed at any one time.

1.6.1.1 32 Switch

The upper limit of the Word counter will be 31 and the lower limit zero for 32 locations when this switch is depressed.

1.6.1.2 64 Switch

The upper limit of the Word counter will be 63 and the lower limit zero when this switch is depressed.

1.6.1.3 128 Switch

The upper limit of the Word counter will be 127 and the lower limit zero when this switch is depressed.

1.6.1.4 256 Switch

The upper limit of the Word counter will be 255 and the lower limit zero when this switch is depressed.

1.6.1.5 512 Switch

The upper limit of the Word counter will be 511 and the lower limit zero when this switch is depressed.

1.6.2 Mode Section

The switches in the Mode section are in three divisions. One division contains switches controlling the programming. They are mechanically interlocked so that only one can be depressed at any one time. The second division controls the speed of programming. They are also interlocked so that only one can be depressed. There can be one switch depressed from each division. The third division contains the MOMENTARY START and STOP switch.

1.6.2.1 Insert Switch

Depressing the INSERT switch will disable the RAM and ROM circuits to prevent loss of the contents of RAM while setting the Word counter or false programming of a ROM while inserting it into the sockets. The Write pulse is disabled.

1.6.2.2 Verify Switch

Depressing this switch allows the operator to verify that the data contained in the selected Input and Output devices are identical. The Write pulse is disabled.

1.6.2.3 Program Switch

This switch must be depressed to write anything into an Output device. When depressed both the Read and Write pulses are enabled.

1.6.2.4 Manual Switch

Depressing this switch allows the operator to cycle through the Word counter one count at a time by cycling the STOP and START switches. If the KEYBD switch is depressed also the Word counter may be controlled by the keyboard keyswitches.

1.6.2.5 Auto Switch

When the AUTO switch is depressed and the STOP/START switches are cycled, the Word counter will count from the present address to the upper or lower limit depending on the direction selected. The keyboard will be disabled with AUTO selected.

1.6.2.6 Start Switch

Depressing the MOMENTARY START switch will transmit a Start pulse to the Control circuits and turn OFF the Stop light.

The counter will advance one count or to either the upper or lower limit depending on the status of the MANUAL and AUTO switches.

1.6.2.7 Stop Switch

Depressing the MOMENTARY STOP switch will transmit a Stop pulse to the Control circuits and turn OFF the Start light. The Stop pulse will stop the Word counter at the location when the switch is depressed.

1.7 CARD INSTALLATION AND CHANGE

CAUTION: **Power should always be removed from the Programmer prior to installing or removing a circuit board from the equipment.**

When power is removed the contents of RAM will be lost and must be reloaded prior to use.

Program and/or Read Only cards are installed in the MEU connectors in the card cage. Since these cards are peculiar to individual PROM's they will have to be changed whenever a different PROM is to be programmed.

A short description of the function of the cards that fit into the MEU connectors follow. (See Section 4, paragraph 4.3.6 for their relative locations.)

1.7.1 **Addmaster Reader/Driver 2 or Addmaster Reader/Driver 3 (J1-M RDR)**
Controls the operation of the Tape Reader and transfers the data input to the system.

In addition the number 3 board controls the operation of the optional Card Reader and enables the ASCII Translator circuits.

1.7.2 **Perf Driver Assembly (J2-M PERF) Programmer I Only**
Provides for transfer of data from the system to the Perforator.

1.7.3 **Program Card One (J3-M PROM 1)**
This connector should contain either a modified Program card or a Read Only card applicable to the particular PROM to be programmed. When programming ROM to ROM this will be the Master position and contain the ROM with the Master program.

1.7.4 **Program Card Two (J4-M PROM 2)**
This connector should have the Program card, applicable to the PROM to be programmed installed. When programming ROM to ROM this will be the Slave position and contain the PROM to be programmed.

1.7.5 **Spare (J5-M SPARE)**
Available for complex programming requirements where an additional Program card is required.

1.7.6 **Translator (J6-M TRANS) (Optional)**
Controls the translation of an ASCII coded tape into binary coded data.

1.7.7 **Ram Buffer Assembly (J7-M RAM)**
Contains the 4K Random Access Memory and the Read/Write controls.

1.7.8 **Address Card Assembly (J8-M ADD)**
Contains the binary address "Word Count" and the circuitry to convert the binary address to the binary coded decimal "Word Count".

1.7.9 **Control Card Assembly (J9-M CONTROL)**
Contains the Master Timing circuits, data buffer, Forward/Reverse selection and Control circuits.

vary with the type of Program or Read Only cards installed and the positioning of the jumpers on the cards.

It is assumed for all operations that the POWER switch is ON and power applied to the Programmer.

NOTE: The ENTRY BAR, ADD FWD and ADD REV keyswitches are all cyclic switches. They should be stroked firmly and immediately released. If they are not released within approximately one quarter second the switch action will be repeated at a cyclic rate of approximately ten operations per second until the switch is released.

1.8.1 Clear Ram

Select KEYBD on the Input section.

Select RAM on the Output section.

Select 512 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET on the Display Panel.

Depress START. The "Word Count" advances to the count of 511. The contents of the RAM have now been cleared and stop occurs.

Select VERIFY on the Mode section.

Depress START. The "Word Count" decreases to the count of 000. This verifies that RAM is cleared.

1.8.2 Keybd to Perf (Programmer I Only)

NOTE: This operation may be used to prepare a tape to be used to program a ROM. It is not recommended since there is no margin for error, that is, there is no capability to correct the tape if an error is made. It is recommended that the Truth Table be inserted into RAM and then after it has been checked and verified, the contents of RAM can be punched by the Perforator.

Select KEYBD on the Input section.

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Word Count" advances to the count 63. The Perforator advances 64 spaces punching only a sprocket hole. This will allow sufficient leader to use with the Tape Reader. Stop occurs at word limit.

Depress RESET to reset the "Word Count" to zero.

Select the desired Data Length.

Select MANUAL on the Mode section.

Depress START.

NOTE: If an Index code is desired in the tape it should be entered at this time with the following steps:

Depress the BIT keyswitches for the selected Index code.

Momentarily (refer to Note paragraph 1.8.2) depress the ENTRY BAR keyswitch. The "Word Count" advances to count 001 and the Perforator punches the Index code.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Depress the desired BIT keyswitches for the zero address on the Truth Table.

Momentarily (refer to Note paragraph 1.8.2) depress the ENTRY BAR keyswitch. The "Word Count" advances to count 001 and the Perforator punches the data entered.

For each address in the Truth Table depress the desired BIT keyswitches and then momentarily the ENTRY BAR. The "Word Counter" should increment one count each time the ENTRY BAR is depressed. If a mistake is discovered prior to entering the data with the ENTRY BAR, the data can be cleared out of the buffers by depressing the WORD CLEAR keyswitch and starting over for that address.

When the selected limit is reached,the "FWD" indicator will go OUT and the "REV" indicator will come ON. Verification cannot be performed automatically since there is no input data to compare against. The Truth Table may be manually verified by comparing it to the punches in the tape.

Depress RESET to reset the "Word Count" to zero.

Select 64 Data Length.

Select AUTO on the Mode section.

Depress START. The "Word Count" advances to the count 63. The Perforator advances 64 spaces punching only a sprocket hole. This will allow the tape to be torn off and leave a trailer. Stop occurs.

1.8.3 Keybd to Ram

This is the recommended method of manually entering data from the keyboard. From RAM it may be output to either the Perforator for permanent storage or to a ROM for programming or both.

If the particular program is ever to be used it should immediately be output into punched paper tape so that is not inadvertently damaged or lost from RAM.

Select KEYBD only on the Input section.

Select RAM on the Output section.

Select the desired Data Length.

Select PROG and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Depress the desired BIT keyswitches for the zero address on the Truth Table.

Momentarily (refer to Note paragraph 1.8.2) depress the ENTRY BAR. The "Word Count" advances to 001.

Repeat the step for each address contained in the Truth Table. If there is no data to be entered at an address, depress the ENTRY BAR without depressing any BIT switches.

The contents of RAM may be visually verified by the following procedure.

Depress RESET to reset the "Word Count" to zero.

Select KEYBD and RAM on the Input section.

Select VERIFY and MANUAL on the Mode section.

Depress START.

Step through each address using the ENTRY BAR comparing the "Data" indicators with the contents of the Truth Table.

NOTE: If the data in any address ***is invalid,*** *correct with the following procedure:*

Select PROG and MANUAL on the Mode section.

Depress the WORD CLEAR keyswitch.

Enter the correct data with the BIT keyswitches and ENTRY BAR.

Select VERIFY and MANUAL on the Mode section.

Momentarily depress ADD REV to verify the correct entry.

Depress ADD FWD to resume for movement and continue verification.

1.8.4 Keybd to Rom

This method is not recommended to program a ROM for the same reason it is not recommended to make a tape. Mistakes cannot be erased.

It may be used to add a data bit or bits in an already programmed ROM.

Select KEYBD on the Input section.

Select ROM (ROM 1 or ROM 2 or ROM 1+2) on the Output section.

Select the desired Data Length.

Select PROG and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Enter the data from the Truth Table with the BIT switches and ENTRY BAR or step to the "Word Count" to be adjusted with the ADD FWD, ADD REV or ENTRY BAR and enter additions.

Verification must be visual by comparing the "Data" lights and the Truth Table.

1.8.5 Reader to Perf

This application may be used to duplicate an existing tape. The only means of verification is to overlay the two tapes and hold them up to a light to compare the punches.

The operational procedure varies if indexing punches are required. The operating instructions for reproducing a tape with or without indexing punches are given below.

1.8.5.1 Without Indexing

Insert the tape to be reproduced in the Tape Reader insuring that part of the blank leader is under the Read Head, and the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Insure that the Tape Reader is turned ON by depressing the MOMENTARY ON switch to ON. The switch is located on the Tape Reader Head on the left side of the Programmer.

Select KEYBD on the Input section.

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Word Count" advances to the count 63. The Perforator advances tape with only the sprocket hole to be used as a tape leader. Stop occurs at word limit.

Select KEYBD and RDR on the Input section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the first bit of data appears on the "Input Data" indicators.

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The "Word Count", Perforator and Tape Reader should step in unison until the "Word Count" reaches the selected count, then stop occurs.

Depress RESET to reset the "Word Count" to zero.

Select KEYBD only on the Input section.

Select 64 Data Length.

Depress START. Perforator advances 64 sprocket hole only tape spaces for a trailer. Stop occurs at word limit.

Tear off the tape and visually verify.

1.8.5.2 **With Indexing**

Insert the tape to be reproduced in the Tape Reader insuring that part of the blank leader is under the Read Head, and the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Insure that the Tape Reader is turned ON by depressing the MOMENTARY ON switch to ON. The switch is located on the Tape Reader Head on the left side of the Programmer.

Select KEYBD on the Input section.

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Word Count" advances to the count 63. The Perforator advances tape with only the sprocket hole to be used as a tape leader. Stop occurs at word limit.

Select KEYBD and RDR on the Input section.

Select the desired Data Length.

Select PROG and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the indexing data appears on the "Input Data" indicators.

Advance the tape one more "Word Count".

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The "Word Count", Perforator and Tape Reader should step in unison until the "Word Count" reaches the selected count.

Depress RESET to reset the "Word Count" to zero.

Select KEYBD only on the Input section.

Select 64 Data Length.

Depress START. Perforator advances 64 sprocket hole only tape spaces for a trailer. Stop occurs at word limit.

Tear off the tape and visually verify.

1.8.6 Rdr to Ram

If more than three identical PROM's are to be programmed at the same time the recommended procedure is to load the data into RAM from the tape and then output it from RAM to ROM. This allows the operator to verify the data on the tape against what is written in RAM without the possibility of damaging a PROM.

This procedure may be followed for three or less PROM's however it will normally require more operating time than programming the PROM directly from a prepared tape.

Tapes are prepared both with and without an Indexing code punched prior to the data for "Word Count" 000. Operating instructions for both types of tape follow.

1.8.6.1 Without Indexing

Insert the prepared tape, to be used in loading RAM, in the Tape Reader. Insure that part of the blank leader is under the Read Head and the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Also that the Tape Reader is turned ON. Depress the MOMENTARY ON switch to

ON. The switch is located on the Tape Reader Head on the left side of the Programmer.

Select KEYBD and RDR on the Input section.

Select RAM on the Output section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the first bit of data appears on the "Input Data" indicators.

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The "Word Count" and Tape Reader step in unison until the "Word Count" reaches the selected count, then stop occurs.

Select VERIFY and AUTO on the Mode section.

Depress START.

The tape should reverse through the Reader and verify that data on the tape and in RAM are identical. Stop occurs at word count Ø.

1.8.6.2 **With Indexing**

Insert the prepared tape, to be used in loading RAM, in the Tape Reader. Insure that part of the blank leader is under the Read Head and the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Also that the Tape Reader is turned ON. Depress the MOMENTARY ON switch to ON. The switch is located on the Tape Reader Head on the left side of the Programmer.

Select KEYBD and RDR on the Input section.

Select RAM on the Output section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the Indexing code appears on the "Input Data" indicators.

Advance the tape one more "Word Count".

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The "Word Count" and Tape Reader step in unison until the "Word Count" reaches the selected count, then stop.

Select VERIFY and AUTO on the Mode section.

Depress START.

The tape should reverse through the Reader and verify that data on the tape and in RAM are identical. Stop occurs at word count Ø.

1.8.7 Rdr to Rom

This method of programming a PROM is the recommended method if programming three or less identical units at the same time.

The Programmer will verify that the tape and programmed ROM contain identical data however there is no capability for correcting the ROM's if an error occurred.

Tapes are prepared both with and without an Indexing code punched prior to the data at "Word Count" 000. Operating instructions for both type of tapes follow.

1.8.7.1 Without Indexing

Insert the programming tape in the Tape Reader insuring that part of the blank leader is under the Read Head and the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Insure that the Tape Reader is turned ON by depressing the MOMENTARY ON switch to ON. The switch is located on the Tape Reader Head on the left side of the Programmer.

Select KEYBD and RDR on the Input section.

Select ROM (refer to paragraph 1.8.2) on the Output section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

NOTE: Insure that the Program card and Interface assembly used correspond with the PROM to be programmed.

Insert the PROM to be programmed into the proper socket.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the first bit of data for "Word Count" 000 appears on the "Input Data" indicators.

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The "Word Count" will advance at a rate equal to the slower of the Tape Reader or programming time rate of the PROM. The "Word Count" will stop when the upper limit is reached. Stop will also occur.

Select VERIFY and AUTO on the Mode section.

Depress START. "Word Count" returns to zero as the tape reverses through the Reader verifying that the data on tape and now programmed ROM are identical. If it stops on any other "Word Count" there is a discrepancy.

1.8.7.2 **With Indexing**

Insert the programming tape in the Tape Reader insuring that part of the blank leader is under the Read Head and the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Insure that the Tape Reader is turned ON by depressing the MOMENTARY ON switch to ON. The switch is located on the Tape Reader Head on the left side of the Programmer.

Select KEYBD and RDR on the Input section.

Select ROM (refer to paragraph 1.8.2) on the Output section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

NOTE: Insure that the Program card and Interface assembly used correspond with the PROM to be programmed.

Insert the PROM to be programmed into the proper socket.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the Indexing code appears on the "Input Data" indicators.

Advance the tape **one** more "Word Count".

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The "Word Count" will advance at a rate equal to the slower of the Tape Reader or programming time rate of the PROM. The "Word Count" will stop when the upper limit is reached and stop occurs.

Select VERIFY and AUTO on the Mode section.

Depress START. "Word Count" returns to zero as the tape reverses through the Reader verifying that the data on tape and now programmed ROM are identical. If it stops on any other "Word Count" there is a discrepency. Stop occurs at word count Ø.

1.8.8 Tran (Translator) to Perf (Optional)

The optional Translator circuits will change an ASCII coded tape into binary information usable in the Programmer, in BNPF or Hexidecimal format.

The only method of verifying a translated ASCII tape is to repeat the procedure and compare the two output tapes. For this reason the recommended method is to enter the data from the ASCII coded tape into RAM so that it may be verified and then output the contents of RAM to the Perforator.

Tapes prepared may be punched either with or without an Indexing code. Instructions for both methods are in the following sub-paragraphs.

1.8.8.1 Without Indexing Code

The Translator requires use of the Tape Reader located on the left side of the Programmer.

Insert the ASCII coded tape to be translated in the Tape Reader insuring that part of the blank leader is under the Read Head. The narrow portion of the tape, as divided by the sprocket holes, should be to the outside of the Reader. Insure that the Tape Reader is ON by depressing the MOMENTARY ON switch on the Tape Reader Head to ON.

Select KEYBD only on the Input section.

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The tape advances perforating sprocket holes only to provide a blank tape leader.

Select KEYBD and TRAN on the Input section.

Select PERF on the Output section.

Select the desired Data Length.

*Select INSERT and MANUAL on the Mode section.

*Depress RESET to reset the "Word Count" to zero.

*Depress START.

*BNPF only.

*Momentarily (refer to Note paragraph 1.8.2) depress the ENTRY BAR. The Reader advances until it reads the first data bit. The "Word Count" advances to 001.

*Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The Tape Reader advances the ASCII coded tape, the Perforator punches and the "Word Count" advances for each data word entered until the selected upper limit is reached. Stop occurs.

Select KEYBD only on the Input section.

Select 64 Data Length.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances punching only sprocket holes to provide a blank trailer for the tape. Stop occurs at word limit 63.

Tear off the tape.

If verification is desired, repeat the procedure and compare the two output tapes from the Perforator.

1.8.8.2 **With Indexing Code**

The Translator requires use of the Tape Reader located on the left side of the Programmer.

Insert the ASCII coded tape to be translated in the Tape Reader insuring that part of the blank leader is under the Read Head. The narrow portion of the tape, as divided by the sprocket holes, should be to the outside of the Reader. Insure that the Tape Reader is ON by depressing the MOMENTARY ON switch on the Tape Reader Head to ON.

Select KEYBD only on the Input section

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The tape advances perforating sprocket holes only to provide a blank tape leader.

Depress RESET to reset the "Word Count" to zero.

Select PROG and MANUAL on the Mode section.

*BNPF only.

Depress START.

Enter Indexing code with the BIT keyswitches.

Depress Space Bar. Perforator punches Indexing code. "Word Count" advances to 001.

Select KEYBD and TRAN on the Input section.

*Select INSERT and MANUAL on the Mode section.

*Momentarily (refer to Note paragraph 1.8.2) depress the ENTRY BAR. The ASCII tape advances until the first data character is entered. The "Word Count" advances to 002.

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The Tape Reader advances the ASCII coded tape, the Perforator punches and the "Word Count" advances for each data word entered until the selected upper limit is reached, where stop occurs.

Select KEYBD only on the Input section.

Select 64 Data Length.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances punching only sprocket holes to provide a blank trailer for the tape. Stop occurs at word count 63.

Tear off the tape.

If verification is desired repeat the procedure and compare the two output tapes from the Perforator.

1.8.9 Tran (Translator) to Ram (Optional)

This is the recommended method of operation for the optional Translator circuits since there is a verifying capability.

Select KEYBD and TRAN on the Input section.

Select RAM on the Output section.

Select the desired Data Length.

*Select INSERT and MANUAL on the Mode section.

*Depress RESET to reset the "Word Count" to zero.

*Depress START.

*BNPF only.

*Momentarily (refer to Note paragraph 1.8.2) depress the ENTRY BAR. The Tape Reader advances until the first data character is entered into the buffers. The "Word Count" advances to 001.

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The Tape Reader and "Word Count" advance until the upper limit of the selected Data Length is reached.

To verify, reinsert the ASCII coded tape into the Tape Reader at the beginning.

Depress RESET to reset the "Word Count" to zero.

*Select INSERT and MANUAL on the Mode section.

*Depress START.

*Momentarily (refer to Note paragraph 1.8.2) depress the ENTRY BAR. The Tape Reader advances until the first data character is entered into the buffers. The "Word Count" advances to 001.

*Depress RESET to reset the "Word Count" to zero.

Select VERIFY and AUTO on the Mode section.

Depress START. The Tape Reader advances comparing the data on the ASCII coded tape with the contents of RAM. The Reader and "Word Count" stop when the upper limit of the select Data Length is reached. If the "Word Count" stops at any other count the tape and RAM are not identical and do not verify.

1.8.10 Ram to Perf (Programmer I Only)

This operation is used to obtain a permanent record of a program. The data on RAM may be obtained from any available source. Operating instructions for standard with-count the tape and RAM are not identical and do not verify. Stop occurs at word limit.

1.8.10.1 Standard Operation

Select KEYBD only on the Input section.

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances punching sprocket holes only to provide a blank leader for the tape.

Select RAM on the Input section.

*BNPF only.

Select the desired Data Length.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Word Count" and Perforator advance in unison to the upper limit of the "Word Count" with the Perforator punching the data from RAM into the tape.

Select KEYBD on the Input section.

Select 64 Data Length.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances 64 sprocket holes only providing a blank trailer for the end of the tape. Stop occurs at word count 63.

Tear off the tape and store.

NOTE: If verification of the new tape is desired, continue the operation as follows.

Insert the tape to be verified in the Tape Reader located on the left side of the Programmer. Insure that part of the blank leader is under the Read Head and that the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Depress the MOMENTARY ON switch on the side of the Tape Reader to insure that it is ON.

Select KEYBD and RDR on the Input section.

Select RAM on the Output section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the data contained in "Word Count" zero appears on the "Input Data" indicators.

Depress RESET to reset the "Word Count" to zero.

Select VERIFY and AUTO on the Mode section.

Depress START. The Reader and "Word Count" advance in unison to the selected upper limit. If the "Word Count" stops at any other location the tape and contents of RAM are not identical and verification did not occur. Stop occurs at word limit.

1.8.10.2 Insert Indexing

Select KEYBD only on the Input section.

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances punching sprocket holes only to provide blank leader for the tape.

Select the desired Data Length.

Select PROG and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Enter the Index code using the BIT keyswitches.

Depress space bar.

Select RAM on the Input section.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Word Count" and Perforator advance in unison to the upper limit of the "Word Count" with the Perforator punching the data from RAM into the tape. Stop occurs at word limit.

Select KEYBD on the Input section.

Select 64 Data Length.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances 64 sprocket holes only providing a blank trailer for the end of the tape. Stop occurs at word count 63.

Tear off the tape and store.

NOTE: If verification of the new tape is desired, continue the operation as follows.

Insert the tape to be verified in the Tape Reader located on the left side of the Programmer. Insure that part of the blank leader is under the Read Head and

that the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Depress the MOMENTARY ON switch on the side of the Tape Reader to insure that it is ON.

Select KEYBD and RDR on the Input section.

Select RAM on the Output section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the Indexing code appears on the "Input Data" indicators.

Advance the tape **one** additional "Word Count".

Depress RESET to reset the "Word Count" to zero.

Select VERIFY and AUTO on the Mode section.

Depress START. The Reader and "Word Count" advance in unison to the selected upper limit. If the "Word Count" stops at any other location the tape and contents of RAM are not identical and verification did not occur. Stop occurs at word limit.

1.8.11 Ram to Rom

The program data previously entered into RAM may be output to either ROM 1, ROM 2 or both ROM 1+2. Insure that the correct program and/or Read Only cards and Interface assembly are installed for the ROM to be programmed.

Select RAM in the Input section.

Select the appropriate ROM switch on the Output section.

Select the desired Data Length.

Select INSERT and AUTO on the Mode section.

Place the ROM or ROMs in the appropriate sockets of the Interface assembly.

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section. The ROM blower turns ON.

Depress START. The "Word Count" advances to the upper limit at a rate governed by the ROM being programmed, where stop occurs.

Select VERIFY and AUTO on the Mode section. The ROM blower turns OFF.

Depress START. The "Word Count" steps down to the lower limit verifying that the contents of RAM and the newly programmed ROM are identical. If the count stops at any location prior to the lower limit the ROM does not verify. Stop occurs if verify occurs on all locations of address.

1.8.12 Rom to Perf (Programmer I Only)

This procedure may be used to create a hard copy master tape from a master ROM. The ROM input may be either ROM 1, ROM 2 or ROM 1+2. Insure that the proper program and/or Read Only cards and Interface assembly is installed for the ROM to be read.

The procedure for making a tape with or without an Index code are listed in the following sub-paragraphs.

1.8.12.1 Without Index Code

Select KEYBD only on the Input section.

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances punching sprocket holes only to provide a blank leader for the tape. Stop occurs at word count 63.

Select the appropriate ROM switch on the Input section.

Select the desired Data Length.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Word Count" and Perforator advance in unison to the upper limit of the "Word Count" with the Perforator punching the data from ROM into the tape. Stop occurs at word limit.

Select KEYBD on the Input section.

Select 64 Data Length.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances 64 sprocket holes only providing a blank trailer for the end of the tape. Stop occurs at word limit.

Tear off the tape and store.

NOTE: If verification of the new tape is desired, continue the operation as follows.

Insert the tape to be verified in the Tape Reader located on the left side of the Programmer. Insure that part of the blank leader is under the Read Head and that the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Depress the MOMENTARY ON switch on the side of the Tape Reader to insure that it is ON.

Select KEYBD and RDR on the Input section.

Select the appropriate ROM switch on the Output section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count", advance the tape until the data contained in "Word Count" zero appears on the "Input Data" indicators.

Depress RESET to reset the "Word Count" to zero.

Select VERIFY and AUTO on the Mode section.

Depress START. The Reader and "Word Count" advance in unison to the selected upper limit. If the "Word Count" stops at any other location the tape and contents of ROM are not identical and verification did not occur. Stop occurs at word limit.

1.8.12.2 **Insert Indexing**

Select KEYBD only on the Input section.

Select PERF on the Output section.

Select 64 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances punching socket holes only to provide blank leader for the tape. Stop occurs at word limit.

Select the desired Data Length.

Select PROG and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Enter the Index code using the BIT keyswitches.

Depress space bar.

Select the appropriate ROM switch on the Input section.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Word Count" and Perforator advance in unison to the upper limit of the "Word Count" with the Perforator punching the data from ROM into the tape. Stop occurs at word limit.

Select KEYBD on the Input section.

Select 64 Data Length.

Depress RESET to reset the "Word Count" to zero.

Depress START. The Perforator advances 64 sprocket holes only providing a blank trailer for the end of the tape. Stop occurs at word limit 63.

Tear off the tape and store.

NOTE: If verification of the new tape is desired, continue the operation as follows.

Insert the tape to be verified in the Tape Reader located on the left side of the Programmer. Insure that part of the blank leader is under the Read Head and that the narrow portion of the tape, as divided by the sprocket holes, is to the outside of the Tape Reader. Depress the MOMENTARY ON switch on the side of the Tape Reader to insure that it is ON.

Select KEYBD and RDR on the Input section.

Select the appropriate ROM switch on the Output section.

Select the desired Data Length.

Select INSERT and MANUAL on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Momentarily (refer to Note paragraph 1.8.2) depressing the ENTRY BAR for each "Word Count" advance the tape until the Indexing code appears on the "Input Data" indicators.

Advance the tape **one** additonal "Word Count".

Depress RESET to reset the "Word Count" to zero.

Select VERIFY and AUTO on the Mode section.

Depress START. The Reader and "Word Count" advance in unison to the selected upper limit. If the "Word Count" stops at any other location the tape and contents of ROM are not identical and verification did not occur. Stop occurs at word limit.

1.8.13 Rom to Ram

The program data previously entered into a master ROM may be output to RAM. Insure that the correct Program and/or Read Only cards and Interface assembly are installed for the ROM that is to be used to load RAM.

Select the appropriate ROM switch on the Input section.

Select RAM in the Output section.

Select the desired Data Length.

Select INSERT and AUTO on the Mode section.

Place the ROM or ROMs in the appropriate sockets of the Interface assembly.

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section.

Depress START. The "Word Count" advances to the upper limit and stop occurs.

Select VERIFY and AUTO on the Mode section.

Depress START. The "Word Count" steps down to the lower limit verifying that the contents of RAM and the programmed ROM are identical. If the count stops at any location prior to the lower limit, the RAM does not verify. Stop occurs at word count Ø.

1.8.14 Rom to Rom

The program data previously entered into a master ROM may be output to an unprogrammed PROM. Insure that the correct Program card (PROM 2 position), Read Only or modified Program card (PROM 1 position) and Interface assembly are installed for the PROM to be programmed.

Select ROM 1 on the Input section.

Select ROM 2 on the Output section.

Select the desired Data Length.

Select INSERT and AUTO on the Mode section.

Place the ROM or ROMs in the appropriate sockets of the Interface assembly.

Depress RESET to reset the "Word Count" to zero.

Select PROG and AUTO on the Mode section. The ROM blower turns ON.

Depress START. The "Word Count" advances to the upper limit at a rate governed by the ROM being programmed and stop occurs.

Select VERIFY and AUTO on the Mode section. The ROM blower turns OFF.

Depress START. The "Word Count" steps down to the lower limit verifying that the contents of the master ROM and the newly programmed ROM are identical. If the count stops at any location prior to the lower limit, the ROM does not verify. Stop occurs at Ø limit.

1.8.15 Mark Sense Card Reader to Ram (Optional)

Input from the Card Reader should be Output **only** to RAM. The speed of the Card Reader precludes successful transfer of data to the Perforator or most types of PROMs. The data in RAM may be used immediately to program a PROM or output to the Perforator for a permanent tape record.

Turn the Card Reader LINE POWER switch ON.

Insure that the POWER switch on the side of the Tape Reader is ON.

Select KEYBD and RDR on the Input section.

Select RAM on the Output section.

Select the desired Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START.

Insert the card into the Card Reader. The Card Reader will accept the card and feed it through the Reader.

NOTE: If a Data Length greater than 64 has been selected an additional card will have to be used for each additional 64 characters selected.

Depress RESET to set the "Word Count" to zero.

Select VERIFY and AUTO on the Mode section.

Depress START.

Insert the card or cards, following the original sequence, into the Card Reader. The Card Reader will accept the card and feed it through the Reader. The "Word Count" will advance to the selected Data Length. If it stops at any other "Word Count" it is an indication that the card data does not agree with the ROM data.

If a non-verification occurs, it is necessary to repeat the programming portion of this paragraph before another verify check is performed.

1.8.16 Blank Checking (Verification of an Unprogrammed Prom)

Select KEYBD only on the Input section.

Select the appropriate ROM switch on the Output section.

Select the desired Data Length.

Select INSERT and AUTO on the Mode section.

Insert the unprogrammed ROM into the appropriate socket of the Interface assembly.

Select VERIFY and AUTO on the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Word Count" advances to the upper limit of the selected Data Length. If the "Word Counter" stops at any other count it will be because there is data in the PROM and it is not blank. Stop occurs at word limit.

SECTION 2
PROGRAM (PERSONALITY) CARD INSTALLATION

2.1 GENERAL

Each Programmable Read Only Memory (PROM) available, that the Programmer can program requires the installation of one to three circuit boards peculiar to that particular PROM. Anytime that the operator changes from one type of PROM to another the associated circuit boards must be changed also.

The following sub-paragraphs list the installation procedures for the various types of Program and Read Only cards.

CAUTION: Power should always be removed from the Programmer prior to installing or removing a circuit board from the equipment.

NOTE: All circuit boards are installed with the component side of the board to the right as the operator faces the Programmer.

Cards are installed so that the color coded extractors match the color coded card guides attached to the card cage. Card Position Numbers are read in ascending order from left to right.

All flat cables between cards and the Interface assembly are connected with the red edge of the cable to pin one. Note: Other designations of cable Pin One position may be used from time to time. Cable Pin One should always be matched to connector Pin One regardless of color indication.

2.2 MOS PROGRAM CARDS

The following instructions are used for the installation of Program cards for programming the following PROM's:

- National Semiconductor MOS (all)
- Intel MOS (all)
- Micro Systems International MOS (all)

Install the Read Only MOS card (optional) in Card Position 3. Connect flat cable between the 26 pin connector on the card and the number one pin on the ROM 1 socket of the Interface assembly.

The MOS Program cards consist of two cards cabled together with a 16 pin flat cable.

Install the MOS card one (brown extractor tab) in Card Position 4.

Install the MOS card two (white extractor tab) in Card Position 5.

Connect the 26 pin flat cable between the 26 pin connector on MOS card two in Card Position 5 and the number two connector of ROM 2 socket on the Interface assembly.

2.3 FUSIBLE LINK PROGRAM CARDS (SINGLE CARD CONFIGURATIONS ONLY)

Install the Read Only card (optional) in Card Position 3. Connect the card to the ROM 1 socket on the Interface assembly with the 26 pin flat cable.

Install the Program card in Card Position 4. Connect the card to the ROM 2 socket of the Interface assembly with the 26 pin flat cable.

2.4 AVALANCHE INDUCED MIGRATION PROGRAM CARDS (OLD STYLE)

These procedures are applicable for the following Program cards:

- Intersil 5200
- Intersil 5203A

These cards are physically mated at the factory to form a set. They should only be separated by qualified service personnel.

Install as a set in Card Positions 3 and 4 with the component side to the right when facing the Programmer. A Connector assembly is positioned between the two cards. Connect the front 26 pin connector to ROM 1 socket and the rear connector to the ROM 2 socket of the Interface assembly with the flat cable provided.

2.5 BIPOLAR PROGRAM CARDS (CARD SETS, NEW STYLE)

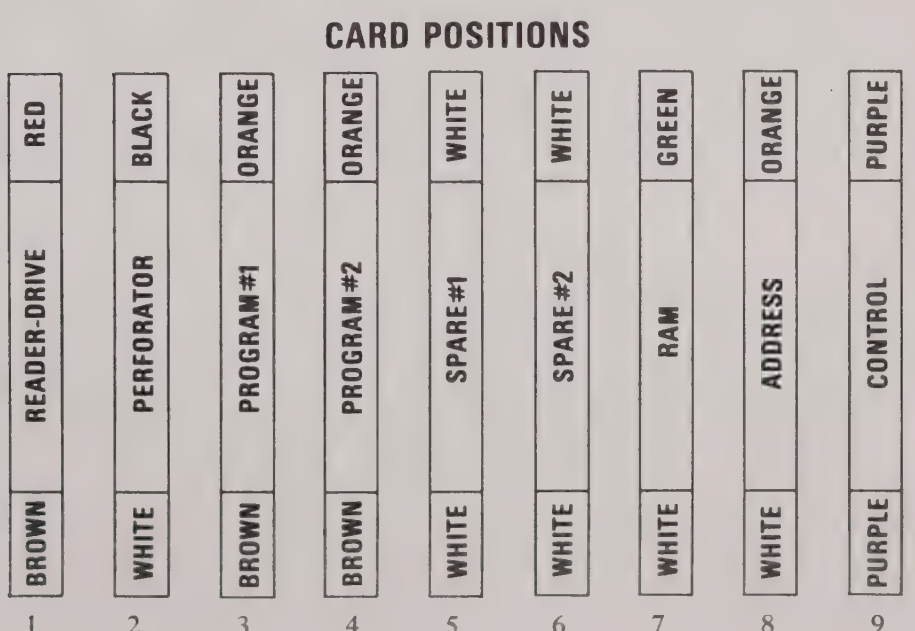
These cards are designed such that all program functions are contained on a card set consisting of two cards cabled together with a 16 pin flat cable. The number one card (brown extractor tab) is referred to as the digital card. The number two card (white extractor tab) is referred to as the analog card.

Install the number one (digital) card (brown extractor tab) in Card Position 4.

Install the number two (analog) card (white extractor tab) in Card Position 5.

Connect the 26 pin flat cable between the 26 pin connector on card two (analog) in Card Position 5 and the number two connector of ROM 2 socket on the interface assembly.

Read only cards are installed in Card Position 3 as described under 2.3.



SECTION 3

POWER SUPPLY

3.0 Power Supply

3.1 General Description

The Power Supply converts the A.C. line voltage of 115/230 volts + 10%, 50-60 Hertz, single phase, into the six D.C. voltages required by the Data I/O Programmer. These voltages, +5, -9, -5, +24, + Programmable, and the floating 48 volt supply are all controlled by 723 Precision Voltage Regulators. Each circuit is set up with current limiting and short circuit protection. The Power Supplies limit at the following currents:

+5	.5 Amperes
-9	.500 Milliamperes
-5	.250 Milliamperes
+24	1.2 Amperes
+ Programmable	1.2 Amperes
Floating 48 Volts	1.0 Amperes

3.2 Power Supply Operation

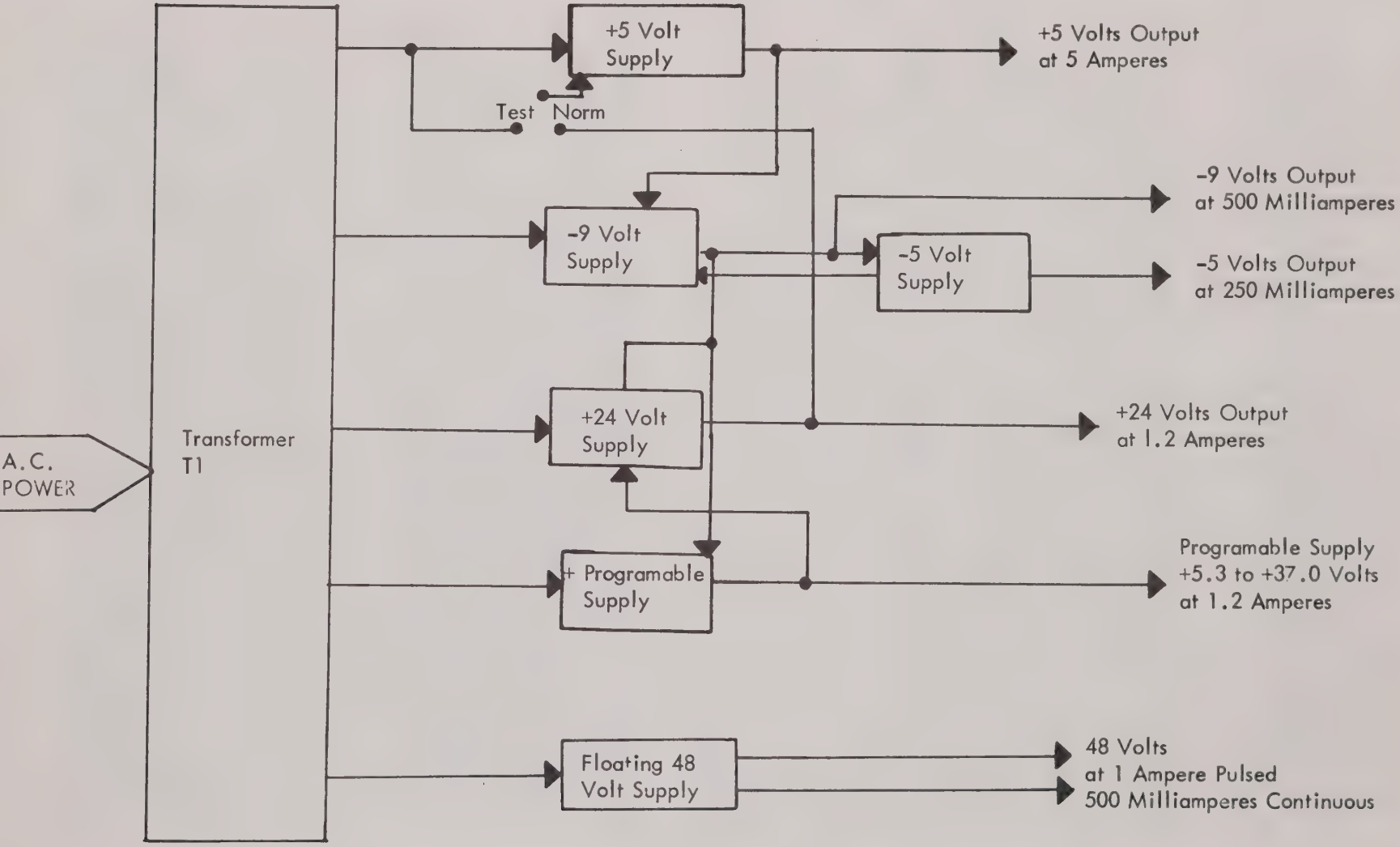
(Refer to schematic 1087)

3.2.1 Short Circuit Protection

The +5, -9, -5, +24 and +Programmable Supplies are interconnected as shown in the block diagram on the following page. As a result of this type of loop, one voltage is dependent on another voltage to ensure that the voltage remains at its proper voltage level. Therefore, a short on any voltage output to ground will shut down the next voltage in the loop until all of the voltages are shut down. This provides protection for the power supply against supplying maximum current for any length of time. After the short has been removed the Power Switch has to be switched off; after the capacitors have discharged, switch back to on to start the power up sequence. A test jumper has been provided to open the interconnecting loop for troubleshooting.

3.2.2 +5 Volts

A.C. current flows through the Primary windings of the transformer T1 when the Power Switch is in the On Position. The voltages are then developed on the secondary windings of the transformer; 9 volts RMS at 5 amperes across the blue leads, 10.5 volts RMS at 1 Ampere across the violet leads, 33 volts RMS at 1.5 Amperes across the yellow leads, and 50 volts RMS at 750 Milliamperes across the white leads. These voltages are applied through J1 to the A.C. inputs of the full wave bridge rectifiers D1, D2, D3 and D4. The D.C. output of D1 charges C13 to 12 volts, the D.C. output of D2 charges C14 to 14 volts, the D.C. output of D3 charges C15 to 70 volts, and the D.C. output of D4 charges C16 to 45 volts. As the voltage increases across C16, capacitor C18


A.C.
POWER
Transformer
T1
+5 Volt
Supply
Test
Norm
+5 Volts Output
at 5 Amperes
-9 Volt
Supply
-9 Volts Output
at 500 Milliamperes
-5 Volt
Supply
-5 Volts Output
at 250 Milliamperes
+24 Volt
Supply
+24 Volts Output
at 1.2 Amperes
+ Programable
Supply
Programable Supply
+5.3 to +37.0 Volts
at 1.2 Amperes
Floating 48
Volt Supply
48 Volts
at 1 Ampere Pulsed
500 Milliamperes Continuous

is charged to provide a voltage ot the +V and Vcc inputs of the 723 of the +5 volt supply (U1) through the Jumper (JP1) in the "NORM" position. When the voltage at +V of U1 exceeds 9 volts, the 723 will operate providing a reference voltage of 7 volts at U1 Pin 6 and 2.5 volts at Pin 5 of U1 through the voltage divider R17 and R19. This causes the output voltage of the 723 to increase supplying base current to Q10 and Q10 supplies base current to series pass transistor Q1. As the voltage on Q1 emitter increases, the voltage on Pin 4 of U1 increases to 2.5 volts switching off the 723. The voltage divider of R15, R16 and potentiometer R18 is set up to supply a voltage of 2.5 volts on Pin 4 of U1 when Q1 emitter is 5.2 volts.

3.2.3 -9 Volts and -5 Volts

The +5 volts then supplies the voltage for the +V input of the -9 regulator (U2) causing the device to start regulating and Q2 to draw base current. Q2 turning on provides a ground reference for the -9 volt supply. The voltage on Pin 7 of U2 will become more negative as Q2 is turned on harder. Zener diode CR1 will clamp the voltage on the base of Q3 and Pin 4 of U2 at -5.6 volts. The base emitter junction of Q3 will drop .6 volts charging C1 to -5 volts. The inverting input at U2 Pin 4 being at -5.6 volts is used as a reference for the -9 regulator. The voltage divider of R7, R6 and potentiometer R40 is set up to have a voltage of -5.6 volts on Pin 5 of U2 when the minus side of the supply is at -9 volts.

3.2.4 + Programmable

With C16 charged to 45 volts and the -9 volt supply not at -9, current will flow through R44 and R43 to the base of Q4 and Q5, turning these two transistors on will hold pins 13 of U4 and U5 at ground, preventing the internal output transistors of U4 and U5 from turning on, therefore holding off the +24 volts and the + programmable supplies. When the -9 volt supply reaches -9 volts, the divider of R43 and R10 will cause the base of Q5 to go to -0.6 volts causing Q5 to switch off. This releases the internal output transistor of U5 and allows the voltage of the programmable supply to increase. The voltage divider of potentiometer R30, R9 and R8 is set up to provide a voltage of 5.3 volts on Pin 5 of U5 therefore, the programmable supply will increase to 5.3 volts with the sense and operate lines left open. When a program card is plugged into the Data I/O Programmer requiring a specific voltage, a resistor (Rxx) on the program card is either connected from the operate line to ground or from the sense line to the operate line and the operate line is tied to ground. This will set up a voltage divider with R3, R2, R1 and Rxx, requiring the voltage at Q8 emitter to increase to a specific voltage between 5.3 volts and 37 volts depending on Rxx value and how it is connected (See Fig. 1) to maintain 5.3 volts on Pin 4 of U5.

3.2.5 +24 Volts

A the programmable supply voltage becomes more positive, current will flow thorugh R38 and Q13 base, turning Q13 on and switching Q12 off. With Q12 off and Q4 off, U4 pin 13 is allowed to go positive turning the internal output transistor of Q4 on. This allows the 723 to drive Q7 causing the emitter to go

positive, as Q7 emitter voltage increases, the voltage at U4 Pin 4 increases through voltage divider R27, R25 and R26 until the voltage at Pin 4 of U4 is the same as U4 Pin 5. The voltage divider is set up so Q7 emitter will be 24 volts at this time. The 24 volts on Q7 emitter will supply the voltage through CR4 to the +V input of U1 preventing the supply from shutting down after C18 has discharged.

3.2.6 48 Volts

The floating 48 volt supply is isolated from the reset of the power supply and is not referenced to ground until J2 Pin 9 is connected to ground providing -48 volts at J2 Pin 5 or connecting J2 Pin 5 to ground providing +48 volts at J2 Pin 9. The floating 48 volt supply comes up independent of the other voltages. The D.C. output charged C15 to 70 volts, current flows through R20 and Zener diode CR2 clamping the voltage at +V and Vcc inputs of U3 to 24 volts. The output of U3 drives the base of Q9 which allows Q9 to sink base current from Q6, turning Q6 on until the collector reaches 48 volts. At 48 volts the voltage divider R12 and R23 provide a voltage on Pin 4 of U3 that will equal the voltage on Pin 5 of U3 resulting from the voltage divider R21, R22 and the adjustment of potentiometer R24. A current is drawn from the 48 volt supply, voltage is dropped across R31, if the current increases to 1.2 amperes the voltage across R31 turns on Q11 allowing current to flow through R32 and through the current limit circuitry of U3 causing the output voltage to decrease. This will continue until the current is decreased or F2 opens up protecting the components of the floating 48 volt supply from breaking down or damage due to excess heat.

PROGRAM SUPPLY OUTPUT
AS A FUNCTION OF Rxx
WITH RESISTOR CONNECTED
FROM OPERATE TO GROUND

Rxx	Voltage
0 ohms	21.6
1000 ohms	18.8
2000 ohms	16.8
3000 ohms	15.3
4000 ohms	14.2
5000 ohms	13.2
6000 ohms	12.5
7000 ohms	11.9
8000 ohms	11.3
9000 ohms	10.9
10000 ohms	10.5
12000 ohms	9.8
15000 ohms	9.1
20000 ohms	8.3
30000 ohms	7.3
40000 ohms	6.8
50000 ohms	6.4
100000 ohms	5.7
200000 ohms	5.3

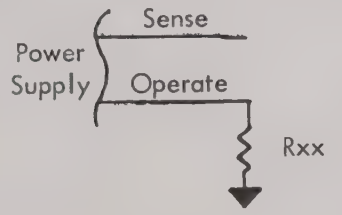


TABLE 3.1

PROGRAM SUPPLY OUTPUT
AS A FUNCTION OF Rxx
WITH RESISTOR CONNECTED
FROM SENSE TO OPERATE
WITH OPERATE GROUNDED

Rxx	Voltage
0 ohms	38.6
10000 ohms	33.5
11000 ohms	32.4
12000 ohms	31.5
13000 ohms	30.7
14000 ohms	30.1
15000 ohms	29.5
16000 ohms	29.0
17000 ohms	28.5
18000 ohms	28.2
19000 ohms	27.8
20000 ohms	27.5
25000 ohms	26.3
30000 ohms	25.5
35000 ohms	25.0
40000 ohms	24.6
45000 ohms	24.2
50000 ohms	24.0
60000 ohms	23.6
90000 ohms	22.9
500000 ohms	21.8

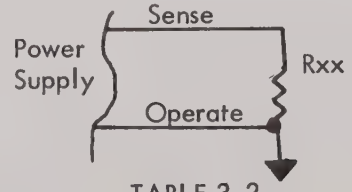


TABLE 3.2

SECTION 3
FUNCTIONAL DESCRIPTION

3.1 GENERAL

This discussion will be by Logic board, in the sequence a character would pass through the logic enroute from Input device to Output device. Each Logic board description will be further broken down into individual operations that occur on the board. This will provide a Format which may easily be referenced for any operation on any Logic board. Reference may be made to the System Block Diagram (018-11837) for an overall view of the system operation.

Operation of the Programmer I and Programmer II systems is identical except for the Perforator and Perf Driver circuits. These circuits are not included in the Programmer II model.

The section contains descriptions on the two Reader Driver boards (Addmaster No. 2 and Addmaster No. 3). Only one version of each board will be present in each Programmer. Each board should be carefully checked for part number to insure that the applicable description has been selected. Reader Driver Addmaster No. 3 must be installed if the optional ASCII Translator card or Mark Sense card Reader are to be used.

3.2 POWER SUPPLY ASSEMBLY (203-24125)

The wiring for the AC power supply is shown in this drawing. The power supply can be connected to accept an input either 110 or 220 volts AC.

RESCINDED

If 110 volts is the required input pin 2 of TB1 will be connected to pin 3 and pin 4 will be connected to pin 5. The results is that the two primary windings of power transformer are connected in parallel.

If 220 volts is the required input pin 3 of TB1 will be connected to pin 4. The result connects the two primary windings section of the power transformer in series. Since all of the system accessory motors are wired for 110 volt operation the input must be center tapped from the input windings of the power transformer if 220 volts is applied as an input.

Power is applied to the power transformer primary windings through fuse F1, the POWER switch and TB1.

One secondary output is rectified by BR1 and its associated filter network to provide $\pm$45 volts to Modular Power Supply cards. The other secondary outputs 48 volts AC to the Modular Programmable Power Supply.

3.3 MODULAR POWER SUPPLY MEU CONNECTOR ASSEMBLY (201-24532)

This drawing lays out the wiring and connectors for mounting the Modular Power Supply boards. Outputs to the system are taken by hard wire from the tie points shown beside the connectors to J5 through J9 on the Power Supply assembly.

3.4 MODULAR +5 VOLT POWER SUPPLY (201-24528)

The Power Supply board contains a 20KHz oscillator and a switching regulator supply. The oscillator output is used on this board and on the +24 volt Modular Power Supply.

3.4.1 Oscillator

The NE555 Timer (U2) is connected in an astable mode to provide a controlled oscillator at approximately 20KHz. The frequency of the oscillator is controlled by the values of C1, R6 and R14. The output is used on both the +5 and +24 volt regulators.

3.4.2 Reference Volt

The plus and minus 45 volt signals are brought in from the power supply on Pads 14 and 15 respectively. The +45 is dropped to 6.2 volts by the zener CR3 and adjusted by the voltage divider R16 and R12 for a +5 volt reference. The -5 volt reference is dropped from the 45 volts by zener CR2 to 6.2 volts and adjusted with the divider R15 and R3.

3.4.3 Plus 5 Volt Supply

The output of the oscillator is integrated by C4/R9 and applied to U1 voltage comparator at pin 3 as a triangular waveform riding on a 5 volt reference. This will cause U1 to turn ON and OFF and provide the switching into the transistor Q1 to keep a level +5 volt output. The L1/C6/C7 network will filter the output of the transistor. CR4 provides protection for the +5 circuits. If the output exceeds 6.8 volts the output will be clamped to ground which will result in the +45 volt supply line fuse burning out. This will prevent damage to the +5 volt supply circuit components.

3.5 MODULAR +24 VOLT POWER SUPPLY ASSEMBLY (201-24526)

This assembly supplies the Programmer with a -5, -9 and +24 volts.

REVISED

3.5.1 Minus 9 and Minus 5 Volt Regulator

The clock is input, integrated, applied to the -5 reference and applied to the voltage comparator as a triangular waveform. It is compared with the output and U1-1 outputs a switching signal to the transistor Q1. This is filtered and output on Pad N as the -9 volt supply. The zener CR4 will clamp the output to ground when the output rises above 12 volts to burn out the -45 volt supply fuse and prevent damage to the -9 volt supply components. The -9 output will be divided by R13 and the 5.1 volt zener CR3 to provide the input to Q2 which will output a -5 volt supply.

3.5.2 Plus 24 Volt Regulators

The clock is input, integrated and applied with the +5 reference to one side of the voltage comparator U2 which is turned ON and OFF to provide a switching voltage to the transistor Q3. The result is filtered and output to the system on Pad P for use in the Perforator and Paper Tape Reader.

3.6 MODULAR PROGRAMMABLE POWER SUPPLY ASSEMBLY (201-23530)

This assembly contains a positive and a negative Programmable Power Supply. The exact voltage output is set up by placing a resistive load in parallel with the voltage divider circuits on this board. The added resistors will be located on the ROM Program cards and will output any selected voltage required and not supplied by the other assemblies. Both regulators operate as linear regulators.

3.6.1 Positive Regulator

The output value will be determined by the resistive load in the ROM Program card which will be applied between Pads J and K. This resistive load will be in parallel with the R2/R3 series and in series with R4 to form a voltage divider and apply the selected voltage to one side of the U1 op amp. A +5 reference will be applied to the

other side of the op amp. U1 will sense any variation in the output voltage and will use this variation to vary the amount of conduction of the transistor Q1. An output of +22 to +35 volts can be obtained with effective regulation.

3.6.2 Negative Regulator

Supply voltage for the negative regulator is an AC voltage from the Power Supply assembly of approximately 48 volts. The required resistive load will be input from the ROM Program card between Pads M and N. The resultant voltage from the voltage divider network will be input to the U2 op amp and compared with the output for any variation. The amount of variation will affect the conduction of transistor Q2. Outputs up to minus 65 volts can be obtained with effective regulation.

3.7 AC MOTOR CONTROLLED ASSEMBLY (201-24607)

This board is used to apply 110 volt AC operating voltages to the Perforator or ROM fan, when one is selected as the Output device by the Control Switch assembly and PROGRAM has been selected. When one of the ROM positions is selected by depressing the appropriate switch on the Control Switch assembly, a LOW will be input on Pads 9 and K which will energize the Relay K2. The energized relay will output on Pads 12 and N the applied AC voltage to the ROM fan. If the PERF switch is depressed a LOW will be input on Pads 10 and L to energize K1 which will output the applied AC voltage to the Perforator Motor on Pads 11 and M. Depressing any other switch will automatically remove the voltage from the Accessory Motor.

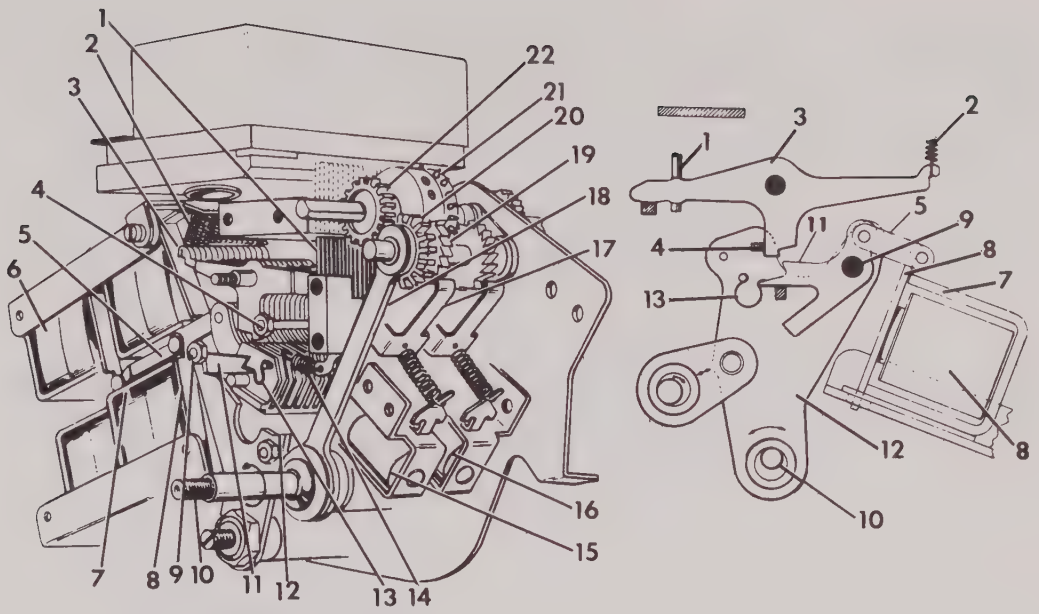
3.8 PERFORATOR

Power is applied to the motor of the Punch when PERF is selected on the Control Switch assembly and PROG is selected on the Mode Switch assembly. This applied power causes the Input Eccentric Shaft (10) to rotate in the indicated direction and imparts motion to the Punch Pawl Yoke (12).

When a code is presented to the Perf Driver it will output to the Punch which will cause the appropriate Punch Magnets (6) to be energized and move the Punch Yoke (12) to the rear of the unit. The pulling action against the Link (5) causes the Punch Pawl (11) to pivot about on the Shaft (9). The end of the Punch Pawl moves up against the tension of the Overcentering Spring (13) until the Pawl is past the center of the Spring, there the Spring tension will push the Pawl into contact with the Punch Driver Arm (3).

As the Yoke (12) and Pawl (11) continue to move rearward,the Punch Driver Arms will pivot up and drive the Punches (1) through the tape to produce the perforated code. The Input Eccentric Shaft (10) continues rotating. The Yoke (12) and Pawls (11) move to the front of the unit and allow the Springs (2) to pull the Driver Arms (3) and Punches (1) out of the tape. Just before the Punch Yoke (12) is fully to the front of the unit the Armature (8) will contact the Magnet Shell (7) and as the Yoke moves to its full forward position the force from the Armature contacting the Shell through the connecting Link (5) pushes the Pawl (11) against the Overcentering Spring until the Pawl is past center and the tension of the Spring returns the Pawl to its inactive or rest position. The Positive Retractor (4) insures that the Punches (1) are withdrawn from the tape should the Springs (2) fail to pull the Punches from the tape. Subsequent rotation of the Shaft (10) and energizing of the Magnets (6) will repeat the punching operation.

Spring (14) is used to eliminate excessive chatter during high speed movement of the Yoke (12).



PUNCH OPERATION
Figure 3.1

During the rotation of the Eccentric Shaft (10), the Index Link (18) moves the rolling Gear (20) up and down over the Index Gear (22). When the Punches are below the platen level and Index Link (18) is at its highest point, the Forward Index Magnet (15), when energized, brings the Interposer (17) into contact with the Ratchet (19).

Once the Interposer (17) has stopped the Ratchet (19) and Gear (20) from turning, the downward motion of the Link is transmitted to the Gear (22) turning it and the Sprocket (21) one space.

When the Sprocket (21) is fully advanced, the Index Magnet (15) is de-energized and the Interposer (17) returns to its rest position by spring tension. The rotation of the Eccentric Shaft (10) raises the Link (18) to its highest point to repeat the preceding operation.

The Perforator has the capability to feed tape in reverse as described in the following paragraph. However this capability is not used in the ROM Programmer.

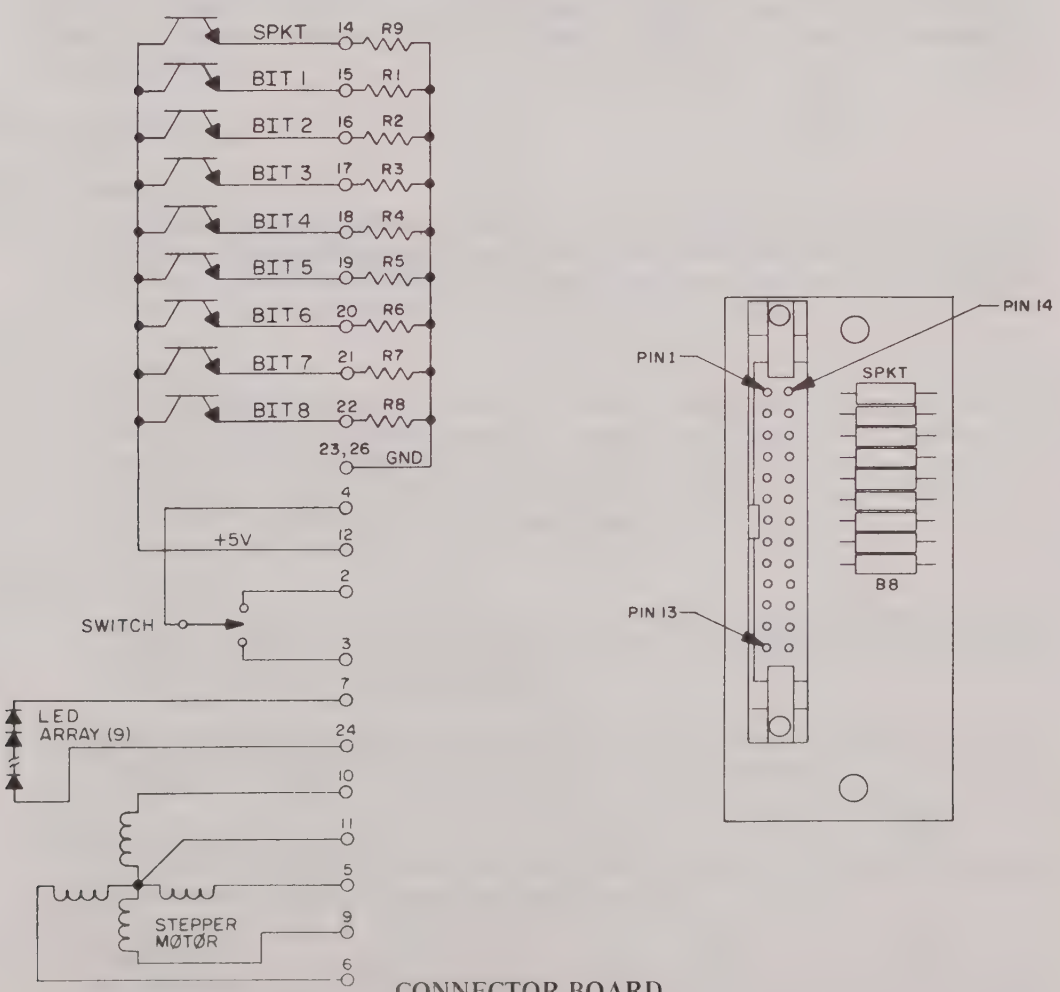
The tape can be fed in the reverse direction by energizing the Reverse Magnet (16). The tape will feed in the same way as described in forward feeding except that the feeding occurs during the upward movement of the Link (18). The punching operation occurs at this time, therefore it is essential that the Punch Magnets (16) are not energized during the Reverse Feed mode.

3.9 TAPE READER ASSEMBLY (104-25548)

The Tape Reader will read standard punched paper tape of at least 50 percent opacity. It may be rolled loosely or fanfolded. The tape is illuminated by infra-red light emitting diodes that are not visible to the eye. This light passes through the, punch for data, hole in the tape and an aperature plate into a photo-transistor array. The resulting photo-current is transformed into TTL logic signals on the Reader Driver assembly.

The small printed circuit board attached to the Reader contains the factory selected gain resistors and a dip connector. The Connector board schematic is shown in Figure 3.2. The photo-transistor array and the selected gain resistors should be changed as an assembly if one is defective.

The tape is incrementally advanced by a sprocket driven by a 4 phase stepper motor. The motor is stepped by energizing sequentially two of the four windings. The Reader will step at approximately 100 characters per second unless controlled by another device of a lesser rate such as the Perforator or Translator.



CONNECTOR BOARD
Figure 3.2

3.10 KEYBOARD SWITCH ASSEMBLY (201-23799)

All switches on the Keyboard assembly are linked to a common point. This point will be LOW through pin 16 only if the AUTO switch on the Mode Switch assembly is open or not depressed and the KEYBD switch on the Control Switch assembly is closed or depressed. If these conditions are met,depressing any of the switches will output a LOW on its respective pin of J1 (J13-M). Data BIT 1 is loaded from S8, DB2 from S7 and on in this manner to Data BIT 8 from S1. The outputs of the keys are utilized on the Control Card assembly.

3.11 CONTROL SWITCH ASSEMBLY (201-24129)

The Control Switch assembly is used to select the devices to be used as inputs and outputs. The Input section is divided into two groups. One group contains only the KEYBD switch. The other the RDR (Reader), TRAN (Translator), RAM, ROM 1, ROM 2 and ROM 1+2. The keys are mechanically interlocked so that only one key from each group can be selected at any one time. Therefore the keyboard can be selected in conjunction with another Input device but no two other devices can be selected together. The Output switches consist of PERF, RAM, ROM 1, ROM 2 and ROM 1+2. These switches are also interlocked so that only one switch can be selected at any one time.

3.11.1 Input Section

3.11.1.1 Key (S1)

Depressing the KEYBD switch will output a LOW at pin 5 of J2 (J11-MEU). This LOW will be routed through the normally closed contacts of the AUTO switch on the Mode Switch assembly and the Control card to enable the keys on the keyboard. It will also turn ON the self-contained indicator light.

3.11.1.2 Rdr (S2)

When the RDR switch is not closed, a LOW that originates through the normally closed contacts of the TRAN switch is output on pin 23 of J2. This LOW output goes to the Tape Reader to insure that it is disabled. When the switch is depressed to close it, the LOW is removed and it allows the Reader to be controlled by the READER ENABLE switch on the Reader itself.

3.11.1.3 Tran (S3)

The TRAN switch outputs a LOW on pin 7 when it is open. This LOW is input to the Tape Reader as an Enabling signal. A LOW is also supplied to the RDR switch as described in the preceding paragraph.

When the switch is closed,a LOW is output on pin 8 to the Translator card and control of the Reader at pin 7 is assumed by the Translator card.

3.11.1.4 Ram (S4)

A LOW is output to the RAM Address assembly on pin 4 of J2,when the RAM Input switch is closed to enable the Read circuitry.

3.11.1.5 Rom 1 (S5)

A LOW is output to the ROM 1 Program card on pin 14 of J2,when the ROM 1 Input switch is closed.

3.11.1.6 Rom 2 (S6)

A LOW is output to the ROM 2 Program card on pin 20 of J2, when the ROM 2 Input switch is closed.

3.11.1.7 Rom 1+2 (S7)

A LOW is output on pins 13 and 17 to both the ROM 1 Program card and the ROM 2 Program card,when the ROM 1+2 Input switch is depressed.

3.11.2 Output Section

3.11.2.1 Perf (S8) .

Depressing the PERF switch in the Output section will output an Enabling signal to the Perf Driver board. The LOW is also inverted at U2-12 and applied to U1-6. If U1-7 has been enabled previously from the PROG switch on the Mode Switch assembly, the LOW at U1-5 will be output on pin 1 of J1 to the AC Motor Controller assembly in the power supply which will output an operating voltage to the Perforator Motor.

3.11.2.2 Ram (S9)

Depressing the RAM Output switch will output a LOW at pin 3 of J2 if either the PROG or VERIFY switches on the Mode Switch assembly have been closed to enable the switch.

3.11.2.3 Rom 1 (S10)

Operation of the ROM 1 switch requires that either the PROG or VERIFY switch on the Mode Switch assembly is depressed to enable contact 5 of the switch, U1-1, and through pin 18 of the Programmable Power Supply. If it is enabled and depressed, a LOW will be output on pin 15 of J2 to the ROM 1 Program card. The LOW will also be inverted and applied to U1-2. The resulting LOW at U1-3 will be output on pin 3 of J1 to the AC Motor Controller assembly in the power supply. An AC operating voltage will be supplied to the ROM fan through a relay on the AC Motor Controller assembly.

3.11.2.4 Rom 2 (S11)

Operation of the ROM 2 Output switch is identical with that of the ROM 1 switch except the LOW output is on pin 21 to the ROM 2 Program card.

3.11.2.5 Rom 1+2 (S12)

Operation of the ROM 1+2 Output switch is identical with that of the ROM 1 switch,except that the LOW output goes from pin 16 to the ROM 1 Program card and from pin 22 to the ROM 2 Program card.

3.12 MODE SWITCH ASSEMBLY (201-24545)

The Mode Switch assembly is used to select the length of the program, the mode of operation and to start and/or stop the cycle of operations. The five Data Length switches are mechanically interlocked to insure that no more than one switch can be depressed or closed at any one time. Depressing one to close it will automatically return or open another switch that had previously been depressed. The Mode switches are divided into two groups. One group consists of the INSERT, VERIFY and PROG switches. The other group the MANUAL and AUTO switches. Each group is mechanically interlocked so that only one switch of that group may be depressed at any time. Both the START and STOP switches are momentary switches. Contact is made only as

long as they are held depressed. If both are depressed simultaneously, the STOP will override. Each switch is discussed individually in the sub-paragraphs following.

3.12.1 Data Length Section

3.12.1.1 512 (S17)

A LOW is applied to pins 1, 2, 3 and 5 of J1 (J14-MEU) if all of the other switches are open. Closing S17 applies a LOW from pins 1 to 4 illuminate the self-contained light in the switch.

3.12.1.2 256 (S16)

Closing S16 will remove the LOW from pin 1 of J1 thus substituting a HIGH signal by opening pins 5-6 and closing 5-8. Closing pins 1-4 will illuminate the self-contained light.

3.12.1.3 128 (S15)

Closing S15 will remove the LOW from pins 1 and 2 of J1 and turn ON the switch light.

3.12.1.4 64 (S14)

Closing S14 will remove the LOW from pins 1, 2 and 3 of J1 and turn ON the switch light.

3.12.1.5 32 (S13)

Closing S13 will remove the LOW from pins 1, 2, 3 and 5 and turn ON the switch light.

NOTE: The HIGH caused by removing the LOW will enable the Data Length decode circuitry on the Control card, select a word limit and prepare the forward/reverse function.

3.12.2 Mode Section

3.12.2.1 Program (S20)

With the PROG switch open a LOW is taken from the Center line and applied from pins 5-6 to pin 9 of J1. This LOW will disable the Write circuitry on the Control card so that a Write output can occur only with the PROG switch depressed. With S20 closed the Write circuitry will be enabled and a LOW will be output on pin 13 of J1 to the Control Switch assembly to be used in the selection of an Output device. Closing the switch will also turn ON the self-contained light.

3.12.2.2 Verify (S19)

Closing the VERIFY switch will insure that the Write circuitry is disabled since the VERIFY and PROG switches are mechanically prevented from being closed simultaneously. When closed, a LOW will be output on pin 14 of J1 to the Control Switch assembly to be used in selecting the Output device to be read to verify. It will also turn ON its self-contained light.

3.12.2.3 Insert (S18)

Closing the INSERT switch itself only turns ON its own light. However, since only one switch of the group can be closed at any one time due to mechanical linkage, the fact that the PROG switch is open will disable the Write circuitry. Also since

both the PROG and VERFIY switches are open, the RAM or ROM output selection circuitry on the Control Switch assembly is disabled. This should prevent inadvertently changing the contents of the RAM or damaging a ROM.

NOTE: This position should always be used when inserting a PROM into the Interface assembly.

3.12.2.4 **Auto (S22)**

With the AUTO switch open a path is provided through the normally closed contacts 5 and 6 to provide a LOW to the keyboard switches from the depressed KEYBD switch on the Control Switch assembly. Closing the switch turns ON the light and removes the path for the LOW thereby disabling the keyboard.

3.12.2.5 **Manual (S21)**

Closing the MANUAL switch removes the LOW from pin 6 of J1. This LOW had gone to the Control card and provided an Enabling signal to the clock that operated the Read/Write/Verify/Address Function decoder. With the HIGH on pin 6 of J1 the Function decoder must be manually advanced for each cycle.

3.12.2.6 **Start (S23)**

Depressing the MOMENTARY START switch will apply a LOW through contacts 5 and 8 to U2-1 to set the U2 latch. The resulting LOW at U2-6 will be amplified by the U1 driver and turn ON the Start light. The HIGH at U2-3 will be output at pin 11 of J1 to the Control card as a Start signal. It will also output at the U1-3 driver to insure that the Stop light is OFF.

3.12.2.7 **Stop (S24)**

Depressing the MOMENTARY STOP switch will apply a LOW through contacts 5 and 8 to U2-5 to reset the U2 latch. The resulting LOW at U2-3 and HIGH at U2-6 will turn ON the Stop light, turn OFF the Start light and output a LOW at pin 11 of J1 to the Control card.

A Stop signal can also be input to the U2 latch from the Control card at pin 12 of J1.

3.13 DISPLAY PANEL (201-23749)

The Display Panel contains indicators, the Word (Address) counter and Word Count (Address) reset. The "Word Count" is a decimal representation of the binary address of the Address Card assembly.

3.13.1 Indicators

There are eight LED indicators (DS1-DS8) for the Input data and eight (DS9-DS16) for the Output data. Two LED's for "Data A" (DS17), the four LOW order Data bits, and "Data B" (DS18), the four HIGH order Data bits. An indicator for "Power Interrupt" (DS19) will come ON when power is reapplied after having been removed. The light will be extinguished when the START switch is depressed. The "Programming" indicator (DS20) will come ON with a Write pulse to inform the operator that data is being written. The two remaining LED's are "Forward" (DS21) and "Reverse" (DS22). A HIGH output from the Control card will be input on pin 21 for "Forward". This will be inverted at U3-4 to illuminate DS21. It will also be inverted at U3-6 to apply a HIGH to the "Reverse" indicator. With a LOW input for

"Reverse", the HIGH at U3-4 will insure that the "Forward" indicator is OFF and the LOW at U3-6 will turn ON the "Reverse" indicator.

3.13.2 Word Counter

The Word counter consists of three solid state numeric display indicators with integrated decoder/drivers. With a BCD logic input from the Address Card assembly of 0-9 the indicator will display the decimal number in its four by seven dot array. The inputs to the IC are: Input 1 = pin 8, Input 2 = pin 1, Input 4 = pin 2, Input 8 = pin 3. A latch enable at pin 5 of the indicator is connected to ground for the required enabling LOW. Pin 4 on the indicator would display a decimal point if enabled with a LOW. Since the decimal function is not used, pin 4 is connected to the +5 volt supply.

3.13.3 Word Count Reset

Depressing S1 on the Display Panel will output a LOW on pin 14 of J2 to the Address card and Control Card assemblies. On the Address card the LOW will reset the address to zero. On the Control card, it will reset the Timing circuits, inhibit the Master Clock and output a LOW to the Mode Switch assembly for a Stop command.

3.14 MEU CONNECTOR ASSEMBLY (PROG. I 201-24093) (PROG. II 201-24927)

This drawing shows the layout of the MEU printed wiring board. It contains the connectors for mounting all the logic boards available for use with the system. In addition, the connectors which link the MEU to the various sub-assemblies are shown. The J10-M socket connects to the Reader. The J11-M to the Control Switch assembly, J12-M to J2 on the Display Panel, J13-M to the Keyboard, J14-M to the Mode Switch assembly and J15-M connects to J1 of the Display Panel. The A and B tie points are connected to the Perforator (201-24093 only) and the E tie points are connected to J5 on the Power Supply assembly.

3.15 READER DRIVER ASSEMBLY, ADDMASTER NO. 2 (201-24569)

This board contains the circuitry for amplifying the outputs of the Photo Array contained in the Reader. The amplified code is then strobed through a set of Data Read Out gates and output on Pads 4 through 11. This output is applied to the device selected as the Programmer output and to the "Input Data" lights on the Display Panel. The board also contains Direction Control circuitry and drivers for the Reader Stepping Motor. The Dip connector J1 is not used in this configuration.

3.15.1 Reader Start

When the READER switch, located on the side of the Reader Head, is depressed to the extreme FORWARD position (MOMENTARY ON) a LOW is input through Pad M to the board. This LOW is applied to the Advance counter to set both stages HIGH at the Q outputs (U16-5 and U16-9). This initializes the Advance counter and enables two and disables two of the four Stepping Motor Driver gates. The Direction memory is also clocked to insure that Forward is selected. At the same time, a HIGH is input at Pad K which enables the other side of all four Motor Stepping Driver gates. The Stepping Motor now has two coils energized and the motor steps once, if the coil combination energized is different from that of the last operation. If not it will remain stationary. The same HIGH is applied to U3-10. The Delete Detect circuitry will apply a HIGH to U3-9 any time that S1 is installed in the grounded position, which is the normal configuration. If not installed, a delete code (data in all levels) will inhibit the transfer of data to the selected output device. Pad P will go HIGH with a Read strobe from the Control card. The resulting LOW at U3-8 will be felt at both U7-11 and 12 provided that S3 is connected from 2 to 3 as required.

The HIGH at U7-13 will strobe all the Data Read Out gates applying the data to Pads 4-11. Either six or eight gates will be strobed depending upon the positioning of jumper S2. Eight levels will be strobed out if S2 is connected 2 to 3 (Normal configuration). With S2 connected in 1 to 2, only six levels will be strobed out on the Output lines.

3.15.2 Reader Advance and Reset

Pads 13 and 15 will reflect the output from the Control card directional circuitry output at Pad 20 of the Control card. HIGH for Forward and LOW for Reverse. Pad 12 is controlled by the TRANS switch and card. If the switch is depressed, the input will be controlled by the Translator card. If the switch is not depressed, the normally closed contacts will apply a LOW to Pad 12 to enable the Forward gate at U5-13, when Forward has been selected by the Control card.

The Forward gate will be strobed with an address incrementing strobe from the Control card at Pad 17. The resulting LOW at U5-11 will insure that the Direction memory is reset for a HIGH at U1-8. This enables U5-4 and U11-13, Direction Control gates, to control the direction of movement of the Reader. The Forward strobe is felt at U3-3 and 4 at the same time. The resulting HIGH at U3-6 will trigger the Test Enable One Shot. The output at U6-13 is inverted at U7-1 and U3-12 to output a HIGH at Pad 16 to the Control card signifying that the Reader is busy. The trailing edge of the Test Enable One Shot pulse will trigger the Busy Delay One Shot for a HIGH going pulse at U6-5. This pulse will continue the Reader Busy at Pad 16 and will clock the Advance counter so that a different set of Stepping Motor Driver gates are enabled and the Reader steps again. This procedure is repeated for each character. The data will be strobed in with the Reader strobe from the Control card and the motor stepped with the Addressing strobe.

The End of Tape circuitry is disabled in the Normal configuration by installing jumper S4 in the 1 to 3 position. If the jumper is installed in the 1 to 2 position a HIGH will be output at U2-9 to disable the Test Enable Single Shot and prevent the Reader from advancing further when a change in level is no longer sensed at pin R to clock the Sprocket memory at U2-3. This change is sensed by the Reader reading the sprocket holes in the tape.

3.16 READER DRIVER ASSEMBLY, ADDMASTER NO. 3 (201-26963)

This board contains the circuitry for amplifying the outputs of the Photo Arrays contained in the Tape Reader and Card Reader. The amplified code is then strobed through a set of Data Read Out gates and output on Pads 4 through 11. This output is applied to the device selected as the Programmer output and to the "Input Data" lights on the Display Panel. The board also contains Direction Control circuitry and drivers for the Reader Stepping Motor. The Dip connector J1 connects to the Card Reader.

3.16.1 Tape Reader Operation

3.16.1.1 Reader Start

When the READER switch, located on the side of the Reader Head,is depressed to the extreme FORWARD position (MOMENTARY ON) a LOW is input through Pad M to the board. This LOW is applied to the Advance counter to set both stages HIGH at the Q outputs (U16-5 and U16-9). This initializes the Advance counter and enables two and disables two of the four Stepping Motor Driver

gates. The Direction memory is also clocked to insure that Forward is selected. At the same time a HIGH is input at Pad K which enables the other side of all four Motor Stepping Driver gates. The Stepping Motor now has two coils energized and the motor steps once, if the coil combination energized is different from that of the last operation. If not it will remain stationary. The same HIGH is applied to U3-10. The Delete Detect circuitry will apply a HIGH to U3-9 any time that JR2 is installed in the grounded position, which is the normal configuration. If not installed, a delete code (data in all levels) will inhibit the transfer of data to the selected output device. The input at U3-11 will be a result of the Exclusive OR action at U11-3. The Pad 12 input to U11-2 is controlled by the TRANS switch on the Control Switch assembly. If the switch is not depressed the normally closed contacts will output a LOW so that a HIGH pulse on Pad P (Read pulse from the Control card) will output a HIGH at U11-3 and combined with the other two HIGH inputs a LOW at U3-8. The LOW at U3-8 will be felt at both U7-11 and 12 provided that JR4 is connected from 2 to 3 as required. The HIGH at U7-13 will strobe all of the Data Read Out gates applying the data to Pads 4-11. If the TRANS switch is depressed the input at Pad 12 will be controlled by the action of the Translator card. The Data Read Out gates will be strobed by the Read pulse at Pad P, if Pad 12 is held LOW by the Translator card or by a HIGH output from the Translator card with an absence of the Read pulse. Either six or eight gates will be strobed depending upon the positioning of jumper JR3. Eight levels will be strobed out if JR3 is connected 2 to 3 (normal configuration). With JR3 connected in 1 to 2, only six levels will be strobed out on the Output lines.

3.16.1.2 Reader Advance and Reset

Pads 13 and 15 will reflect the output from the Control card directional circuitry output at Pad 20 of the Control card. HIGH for Forward and LOW for Reverse. Pad 12 is controlled by the TRANS switch and card. If the switch is depressed, the input will be controlled by the Translator card. If the switch is not depressed, the normally closed contacts will apply a LOW to Pad 12 to enable the Forward gate at U5-13, if Forward has been selected by the Control card.

The Forward gate will be strobed with an Address Incrementing strobe from the Control card at Pad 17. The resulting LOW at U5-11 will insure that the Direction memory is reset for a HIGH at U1-8. This enables U11-4 and U11-9, Direction Control gates, to control the direction of movement of the Reader. The Forward strobe is felt at U3-3 and 4 at the same time. The resulting HIGH at U3-6 will trigger the Test Enable One Shot. The output at U6-13 is inverted at U7-1 and U3-12 to output a HIGH at Pad 16 to the Control card signifying that the Reader is busy. The trailing edge of the Test Enable One Shot pulse will trigger the Busy Delay One Shot for a HIGH going pulse at U6-5. This pulse will continue the Reader Busy at Pad 16 and will clock the Advance counter so that a different set of Stepping Motor Driver gates are enabled and the Reader steps again. This procedure is repeated for each character. The data will be strobed in with the Reader strobe from the Control card and the motor stepped with the Addressing strobe.

The End of Tape circuitry is disabled in the normal configuration by installing jumper JR5 in the 1 to 3 position. If the jumper is installed in the 1 to 2 position, a HIGH will be output at U2-9 to disable the Test Enable Single Shot and prevent the Reader from advancing further when a change in level is no longer sensed at pin R to clock the Sprocket memory at U2-3. This change is sensed by the Reader reading the sprocket holes in the tape.

3.16.2 Mark Sense Card Reader Operation

Data from the Card Reader optical scanner is input on pins 13 through 6 of J1 for levels 1 through 8 respectively. The input is LOW for data as opposed to entry from the Tape Reader. With the exception of the circuits described in the following paragraphs. All operations are identical with those during the Tape Reader operation. The READER ENABLE switch on the Tape Reader must be turned ON to remove the LOW from Pad K before the Card Reader will operate.

3.16.2.1 Card Reader Disable

Pin 5 of J1 controls which portion of the Reader Driver assembly is used. If pin 5 is HIGH, either from the Card Reader or not connected, the LOW at U17-8 will disable the Card Strobe gate at U12-5. It will also be inverted at U17-6 to apply a LOW to Q1 which will cause it to conduct and supply a LOW to the Photo Array LED in the Tape Reader from Pad 18.

Turning ON the Card Reader will apply a LOW at pin 5. This will be inverted at U17-8 to enable U12-5. It also is inverted to LOW at U17-6 to cut OFF the Transistor and disable the Photo Array circuitry in the Tape Reader.

3.16.2.2 Card Reader Strobe

If the Reader has been selected as an input on the Control Switch assembly and the READER ENABLE switch on the Reader is on,a HIGH will be present at Pad K which will enable U12-4. A HIGH will be present at U12-5 when the Card Reader is ON. These two HIGHs combined with the HIGH input at J1 pin 4 normally will output a LOW which will be inverted at U3-12 for a HIGH Reader Busy. The LOW going strobe at pin 4 from the Card Reader will remove the Reader Busy and allow the clock on the Control card to count which will generate a Read pulse and strobe the data through the Data Read Out gates, operate the One Shots and advance the Card Reader in the same way as if operating with the Tape Reader.

3.16.2.3 Mod 32 Counter

The Mod 32 counter counts the number of Data entries. Pin 3 of J1 will go LOW any time that a card is present in the Card Reader. This LOW will remove the Reset from the U18/U19 counter and allow the counter to increment. At the end of the card,pin 3 will go HIGH and reset the counter. When the trailing edge of the Card Reader strobe enables a Reader Busy at U3-12,it clocks the counter at U18-3.

The last strobe on each portion of the card will reset the counter. The HIGH to LOW change at U19-11 will turn OFF Q6 for a period of approximately 300 milliseconds from the action of C29/R19. If jumper JR1 is installed in the "A" position,the resulting HIGH will be inverted at U10-6 to provide an input to the Ready gate and output a Reader Busy. This 300 millisecond period will prevent stray readings while transitioning from the first to the second portion of the card or when removing the card from the Reader.

The counter will be reset and ready to start counting again whether for a new card or the second portion of the same card.

If the Programmer does not utilize a Mark Sense Card Reader, JR1 will be in the "B" position to apply a LOW to the circuit and disable the output of the counter.

3.17 1083 CONTROL CARD ASSEMBLY

The 1083 control card contains the circuitry required to control the various functions of the programmer. Included are the Forward/Reverse control, Data Buffer, Verify control, Mode control and Master Clock and Stroke. Individual circuits will be discussed in the following sub-paragraphs.

3.17.1 Manual Mode Input Control

The information controlled in the Programmer buss structure may be manually or automatically controlled in the 1083 Control Card. When the Control Panel Key is depressed, the system is placed into a holding condition, whereas clock initiation occurs for one cycle, on each depression of the Space Bar for single step, or Slew operation, by depression of the Forward or Reverse key. Motion control circuitry is located in the lower left-hand corner of the drawing 1083. The clock U3 is a NE555 Generator which has for its input on Pin 4, the or'ed inputs of Add Forward, Add Reverse or Space Bar. The Add Forward and Add Reverse keys are applied through Orgate U14 Pin 6 and from there through Gate U3 Pin 3, to enable the input U3 Pin 5 to high. As the output of U9 Pin 3 becomes high, the low pass filter network R2 and C4 allows the Clock to become active prior to the Slew Memory becoming enabled, by a high condition arriving on U15 and 12 and 13. The first Clock pulse will therefore be emitted from U3 Pin 3 immediately upon the threshold being detected at U3 Pin 4. This clock, becoming high, enables the Strobe Pulser U15 Pin 3 to activate the Cycle Hold memory via the Manual Start Gate, U9 Pin 6.

If the add Forward or Add Reverse keys are held in the depressed condition, the following clock pulse arriving out of the Clock Generator U3 Pin 3 will set the Slew memory to on. The actual delay is about 1/2 second, which is controlled by the capacitor C10, and resistor R4. After the Slew memory has been set, the inverter U20 Pin 4 becomes inactive or cut off, thereby effectively placing R24 in parallel with R4, reducing the R content of the RC time constant for the oscillator by a factor of 10. This will cause the free running frequency to be approximately 10 Hz. This may be maintained as long as the Add Forward or Add Reverse keys are held in a depressed condition. As soon as either switch has been de-activated, the gate U9 Pin 3 becomes low, thereby cutting off the clock, resetting the Slew memory and stopping operation.

The manual mode of operation is for one complete cycle of timing functions to be generating with the following hold occurring just before Program.

3.17.2 Space Bar Operation

Space bar, when depressed, turns on inverter U16 and 6 which places a short across C10 and causing the oscillator U3 to be inactive. U3 Pin 3 will therefore follow U3 Pin 4, and single step operation will occur only with the Space Bar. Slewing is not available in this Control Card.

3.17.3 Master Clock and Control Sequence

As Start had occurred, by depressing the Start switch on the control panel in the Manual Mode of Operation, the Cycle Hold memory was immediately set by the Start memory becoming set U10 Pin 5. As this occurred, U10 Pin 6 becoming low is coupled through buffer amplifier U16 Pin 4 to set the Cycle Hold memory on. The Cycle Hold memory becoming on, enables the clock U1 Pin 9 located in the left lower center of the drawing.

The clock, U1 Pin 8, becomes immediately active since other inputs Pin 13, 10 and 12 are all high. The clock is applied directly into the Clock Generator U2 which is a

7490 type counter. This counter provides a timing cycle in such a manner that the Chip Enable to the Control PROM, U4, is enabled when the C output from the counter becomes high. As soon as C becomes low from the input clock being active, U2 Pin 11 becoming high causes the Cycle Counter, U5, to become incremented by the pulse being applied to U5 Pin 5. The Cycle Counter increments only when the Program PROM U4 is de-activated, therefore intermingling of addresses and data spikes is removed. The counter operates in a basic base 16 format and its output applies the address inputs for the lower order four bits of the Control PROM; A, B, C and D inputs. The normal area of Control PROM activity occurs in the upper half of the 32 x 8 PROM, which allows the E input to normally be high. Therefore, the PROM Program starts at location 16.

Sequence of events required from the PROM Program device is first to test for Input Busy, followed by Read, followed by Output Busy Test and then Program. As Program is completed, Verify occurs and following Verify, the Address is incremented and the cycle repeats itself. Jump conditions occur if different activities occur, such as Verify Error or Word Limit.

3.17.4 Input Busy

The Input Busy line from the PROM Control Program U4 exits on Pin 1. The pull up resistor R7 allows the line to be pulled all the way up since it is an open collector device. The reference R into the cable drawing allows the Input Busy pulse to test the Input Busy Gate U11 Pin 11, whose other input, Pin 12, arrives from the Input Reader Driver board, which should normally be in the low condition for not busy to occur. If the input becomes high, the Input Busy Gate becomes true, therefore the output of the gate becoming high, falsifies the Clock Generator U1, via gate U11 Pin 1 becoming low. The system will hold in this condition until the Input Busy function has cleared to a not busy state. If Input Busy is not in a true condition, the Program Control System shall advance to the next clock increment which shall allow Read to occur, exiting on Pin 2 of U4. This pulse becoming low, shall test the Read Advance Gate U14 Pin 13 via gate U11 Pin 10. Pin 8 of that gate again is Input Busy. The output of the Read Gate is applied directly to the output buss Pin X which provides a Read pulse to all devices as long as the Verify memory is in a reset or cleared state. The Read Gate is also presented to the Data Load Gate, which will be discussed under its appropriate heading of DATA I/O Buffer.

3.17.5 Output Busy

Pin 3 of the PROM Control Program U4 is presented following the Read pulse, which is applied to two basic locations. The first location tests the Output Busy Gate U11 Pin 5, located in the lower center of the page, which shall cause the clock to hold if Output Busy is true. The busy pulse is also presented through inverter U7 Pin 6, to test Cycle Stop Gate, U12 Pin 9 and U9 Pin 10. The cycle stop will cause a halt to occur, since Manual is enabled. It occurs because since U9 Pin 10 and 9 are both high at the busy test period, the output of the gate U9 Pin 8 becomes low. As soon as the Output Busy pulse is past, the output of control PROM U4 Pin 3 becoming high falsifies the gate U9 Pin 10. Since the output U9 Pin 8 is trying to become high but still low, held by capacitor C6, the Cycle Stop Gate U12 and 9 and 8 are both low for a finite period of time which passes the pulse out of U12 Pin 10, through orgate U12 11 to cause a Cycle Hold condition. The system will halt at this time prior to Program until the Start switch is either again depressed, or the Forward, Reverse or Space Bar is depressed on the Control Panel. This shall cause a continuation of the program from that point which is the next pulse out called WRITE.

If the program is again started, the Write pulse exists on the U4 Pin 4 to test the Write gate U21 Pin 12 to exit on Pin AA on the buss. During a Write condition, the program personality card shall cause a halt on the buss on Clock Inhibit line Y to directly stop the clock until the program pulse control has been expired. Following

a write pulse, Verify is enabled by U4 Pin 6 becoming low. U4 Pin 6 becoming low passes through inverter U7 Pin 2 to test the Verify memory against the contents of the Verify gates of the Input data and the Data Register, which will be discussed under Verify heading. Following Verify, Pin 9 of U4 is brought to low to cause the increment of the Address to occur. This will occur as long as the Verify memory is in a cleared state, and from that point, Pin 5 is brought to low which is a jump to zero condition to cause the cycle to repeat itself from that point forward. Each depression on the manual mode control of Forward, Reverse of Space Bar, causes one cycle to occur from Program, Verify, Increment Address, back to zero on the program to test for Input Busy Read, Output Busy and halt.

3.17.6 Data Register

The Data Register is located on the left-hand side of the drawing, whose inputs are the DO buss, DO 1 through DO 8 and the outputs are DI 1 through DI 8. The DI register is a transfer memory which allows an input device to present data to the buffer to be memorized so that the buffer can present the data to an output device. This allows, then, the output device to normally display information on the DO buss until a Read pulse occurs, which disconnects that information and presents the input device onto the DO buss, so that the information may then be transferred and memorized from the Data Register and presented out to the DI buss. This allows simultaneous display of the DO and DI buss on the display panel and for Verification.

The Data Register may be set in one of two ways, either manually or by clock control.

3.17.7 Manual Keyboard

The manual keyboard entry system arrives on the lower left-hand edge of the drawing on HH through RR for 8, 7, 6, 5, 4, 3, 2 and 1 key switches from the binary keyboard. Each key directly sets the Data Register only in the Manual mode of operation and is activated only when Start occurs on the control panel. These are direct set inputs to the Data Register which immediately displays that bit on the DI buss on the Display Panel.

The manual keyboard is used for preparing data to be stored into RAM or programming PROMs, for outputting data to a Punch. The normal system operation uses the keyboard to prepare program material from engineer generated code sheets.

3.17.8 Cycle Operation

The Data Load gate U14 Pin 8 tests the clock inputs of the Data Register, which is a transfer pulse to memorize the contents of the DO buss into the Data Register, and present it to the DI buss. This occurs only when the Data Load Gate output becomes high. This occurs during the Read pulse and half way through the Read pulse, the test on the Data Load Gate U14 Pin 9 becomes high from the clock Generator Counter, which then causes a delay test out of the Data Load Gate from the Read pulse. This allows the data inputs on the DO buss to settle to a quiescent state prior to the Data Test pulse occurring.

3.17.9 Verify

Verification is a compare of the contents of the Output Data Register (DI buss) with the inputs of the Data Register, DO buss. It memorizes the data from the input device to the output device, compares them in either a high or low order or both configuration depending on the personality card selected, and the output of the Verify Gates are presented into a Verify memory, to be tested at the proper Verify test time. The High and Low Order Verify Gates are enabled by the Verify Gates U27 Pin 1 and 4 through the A inhibit and the B inhibit inputs (Pin 19 and W on the connector). The high and low order are determined by the personality card set, so that a four bit device, being used in the programmer, only enables the A inhibit input line Pin 19, so that the Low Order Verify Gates only are used. If an eight bit word is used in the program card set, then both A and B inputs are enabled, thereby allowing eight bits to be Verified, one against the other. If a Verify error occurs, the Verify memory, becoming set, inhibits the Read gate U14 Pin 12 and the Input Address Gate U12 Pin 5. This action locks up the system so that no incrementing may occur and a repetitive Read program test function shall cycle until the Verify

condition is cleared. The Verify memory is reset each time the Programming occurs via inverter U7 Pin 6 applied through orgate U27 Pin 8.

3.17.10 Word Limit

Word Limit is a means of determining the end or maximum address that is desired in the system either by a manual selection from the control panel, or automatic selection by the personality card.

Word Limit causes the direction to be reversed in the automatic mode with stop being enabled and in the manual mode, and the direction is reversed. The system attempts to go in Reverse for one clock cycle, but will then see Word Limit once again and appear then to oscillate around the Word Limit condition.

3.17.11 Manual Limit

The Limit Gates, located in the upper left-hand corner of the drawing, have for their inputs the Address lines A5 through 8 for word limit of 32, 64, 128 and 256 conditions, with selection of Word Limit occurring on the manual limit switch inputs Pin 6 F, H and 10. If the Word Limit input 32 is enabled, then Pin 10 is high and all other input Word Limit lines are low, inhibiting the Word Limit gates U29 Pin 8, 3 and 6. As soon as Word Limit Address 32 is reached, which surpasses the actual limit condition of 31, the output of the Limit Gate becomes low, which applies a low condition to the Limit Memory, U13 Pin 2. The Input Busy Test pulse from the Control PROM U4 Pin 1, tests for Input Busy, and also Word Limit and Direction. As the pulse becomes low and returns too high, the Limit memory is set. As it sets, the U13 Pin 5 becoming high causes the jump gate U1 Pin 4 and 5 to become high. Since the Start Memory is on, the jump gate shall cause the Program Control to move into the lower order area of the program sector of the memory, which inhibits Programming and Reading of data. Instead, Input Increment of Address occurs. However, before that can happen, the Direction memory is reversed by the output of the Direction Gate U12 Pin 1 becoming high, testing the binary input of the Direction Memory, U13 Pin 11. The Limit memory will stay in a set condition as long as the "out of limit" condition occurs, therefore the program control will cycle through one sector of its control sequence in the lower order area, which causes the Address Increment to occur in the reverse direction from which Word Limit occurred (reverse). This brings Word Limit back into range, therefore the Limit gates are falsified, allowing the Limit memory input U13 Pin 2 to become high. The next Input Busy Pulse therefore releases or clears the Limit memory, thereby releasing the jump control on the control PROM and returning it to normal program status. The direction of the Direction Memory is now reversed and therefore if the Forward key is again depressed, direction again becomes Forward by reversing the direction from the Manual Direction gates, driving into Word Limit once again and causing an oscillation around the limit area to occur in the *manual mode of operation.*

Any manually preselected limit condition causes the same action to occur only on a higher order of address. Automatic limit from the personality card arrives as a low on Pin CC, which causes exactly the same operation to occur.

3.17.12 Automatic Stop

When the Auto mode is selected, the Autostop gate U21 Pin 8 located at the right center of the drawing is driven to the enabled state by the Limit memory becoming set. This exits on Pin 8 to cause a manual stop to occur, thereby lighting the stop light and halting the system at Word Limit.

3.17.13 Auto Limit Maximum Gates

If the personality card is not inserted into the card slot, two memories cause upper and lower limit control. They are U8 Pin 9 and 6 located in the upper left center of the drawing. These two memories are steered by Forward and Reverse memory and as the upper limit occurs depending upon the jumper of JP1 of expanded memory or standard address card, the Orgate U14 Pin 3 becomes low. This drives the test input of U8 and 11 to high, thereby causing a Forward Auto Limit to occur. This drives the Limit line in CC low, causing an automatic limit and stop to occur in the Forward direction. In the Reverse direction, U8 Pin 2 is enabled to high, therefore as Reverse occurs and Limit reaches zero and down by one location, the Auto Limit memory U8 Pin 6 will set, causing the Word Limit condition and Stop to occur in the Auto condition.

the Function decoder starting at count zero. The first change at U3-6 will clock the master portion of the Limit memory into the slave and output a LOW at U15-10. The counter may now count the extreme position without setting the Limit latch to reset the counters. At the next address a HIGH will be clocked into the Limit memory to reset it for a HIGH at U15-10 and prepare for the next extreme limit address.

3.17.6 Power Interrupt

When power is restored after being removed, the Power Interrupt latch will be set HIGH at U13-6 to turn ON the "Power Interrupt" indicator on the Display Panel.

Depressing the START switch to initiate the Master Clock cycle will reset the Power Interrupt latch for a LOW at U13-6 and turn OFF the "Power Interrupt" indicator.

This light is merely an indication to the operator that power has been removed and the contents of RAM lost. It will have no effect on the operation of the keyboard.

3.18 ADDRESS CARD ASSEMBLY (201-24133)

The Address card consists of two sections. The first is a nine stage Binary counter. The counter will count either UP or DOWN. The second section is a Binary to Binary Coded Decimal (BCD) converter.

3.18.1 Binary Counter

The Binary counter consists of two synchronous 4 bit up/down counters and a JK flip flop connected in series. The JK is the high order bit of the counter.

3.18.1.1 Count Up

To increment the address, a HIGH will be present on Pad 20 from the Control card. This HIGH will enable U8-2 and be inverted at U7-2 to disable U8-12. With an Address pulse on Pad 24 from the Control card, U8-1 will be strobed and the trailing edge of the U8-3 output will increment the counter. The count is output on Pads 1 through 5 and A through D for the LOW through HIGH orders respectively.

3.18.1.2 Count Down

To decrement the counter a LOW will be present at Pad 20. This LOW will disable U8-2 and be inverted at U7-2 to enable U8-12. The next address pulse on Pad 24 from the Control card will result in a strobe at U8-11. The trailing edge will decrement the counter by one and the new address will be sensed on the Output lines.

3.18.1.3 Reset

Depressing the RESET pushbutton on the Display Panel will result in a LOW at Pad 31. This LOW at U3-3 will reset the JK. It will also be inverted at U7-6 and applied to U9-14 and U4-14 to reset the 4-Bit counters. The LOW is also output on Pad DD to the Control card to reset the Timing circuits, inhibit the Master Clock, and routed out to the Mode Switch assembly for a Stop command.

3.18.2 Binary to BCD Converter

The Binary to BCD conversion is done with a SN74185A IC. This chip is derived from a Read Only Memory allowing the conversion in an economical fashion and without the use of adder circuits.

SN74185A TRUTH TABLE
TABLE 3.1

BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E 14	D 13	C 12	B 11	A 10	G 15	Y8 9	Y7 7	Y6 6	Y5 5	Y4 4	Y3 3	Y2 2	Y1 1
0 - 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 - 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 - 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 - 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 - 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 - 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 - 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 - 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 - 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 - 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 - 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 - 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 - 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 - 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 - 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 - 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 - 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 - 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 - 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 - 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 - 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 - 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 - 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 - 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 - 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 - 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 - 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 - 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 - 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 - 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 - 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 - 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = High level, L = Low level, X = Irrelevant

Discussion of this circuit will consist of following the conversion of Binary inputs through to a BCD output. The Truth Table required for these conversions is listed in Table 3.1.

3.18.2.1 **Example 1 (33)**

For an address of 33 the Binary counter would be HIGH at U9-3 and U4-2. All other outputs of U3, U4 and U9 would be LOW. The LSB of the binary and BCD codes are logically equal, therefore the U9-3 output bypasses the converters and is directly output to Pad LL. U2-11 will be HIGH as a result of U4-2 being HIGH. All other inputs to U2 will be LOW. Referring to the Truth Table shows that for this condition Y2 (pin 2), Y7 and Y8 will be HIGH with all other outputs LOW. Y7 and Y8 are not utilized in this circuitry and will not be referred to hereafter. At this time all of the inputs to U6 are decoded and it results in U6-13 HIGH from U2-2 and all other inputs LOW. The Truth Table shows Y4 (pin 4), Y2 (pin 2) and Y1 (pin 1) HIGH and the other three relevant outputs LOW. All inputs to U5 are now decoded. U5-11 and U5-12 are HIGH from U6-1 and U6-2 respectively. U5-10 is LOW from U9-2 and U5-13 from U6-3. The Truth Table shows that this input results in an output of Y1 (pin 1) and Y4 (pin 4) HIGH. Pins 2 and 3 will be LOW. Pads KK and RR are HIGH from U5-1 and U5-4 respectively and Pad JJ and HH LOW from U5-2 and U5-3. The remaining inputs to U1 were also decoded in U6. It resulted in U1-10 HIGH and all other inputs LOW. From the Truth Table this results in U1-1 HIGH out and all others LOW. This will leave Pad PP HIGH and Pads NN, MM, 33, 34 and 35 LOW. At the completion of the conversion Pad LL, KK, RR and PP are HIGH and all other output pads to the Display Panel LOW. Referring to the MEU and Display Panel,this will input a HIGH on pins 4, 3, 8 and 7 of J2 and a LOW on pins 2, 1, 6, 5, 12, 11, 10 and 9 which will decode to display the numbers 033.

3.18.2.2 **Example 2 (170)**

The Binary number equivalent of U9-2, U9-7, U4-2, U4-7 HIGH and U9-3, U9-6, U4-3, U4-6, U3-15 LOW is a decimal 170. This results in an initial configuration of Pad LL LOW, U5-10 HIGH, U6-10 LOW, U6-11 HIGH, U2-10 LOW, U2-11 HIGH, U2-12 LOW, U2-13 HIGH and U2-14 LOW. At this time only the inputs to U2 are available for decoding. From the Truth Table, the U2 inputs result in U2-5 HIGH and all other U2 outputs LOW. There are now LOW inputs to U1-12 and U1-14 and a HIGH input to U1-13 but the other two inputs remain to be decoded. A LOW is input to U6-12, U6-13 and U6-14. All the inputs to U6 are now decoded and from the Truth Table it results in U6-1 LOW, U6-2 HIGH, U6-3 LOW, U6-4 LOW and U6-5 LOW. All of the remaining inputs are now decoded for U1 and U5. From the Truth Table U5 will decode for a LOW at U5-1, LOW at U5-2, LOW at U5-3 and HIGH at U5-4. A HIGH will be decoded at U1-1, HIGH at U1-2, LOW at U1-3, HIGH at U1-4, LOW at U1-5 and LOW at U1-6. All of this will result in Pads RR, PP, NN and 33 HIGH and Pads LL, KK, JJ, HH, MM, 34 and 35 LOW. This will decode in the Display Panel to display the decimal number 170.

3.18.2.3 **Example 3 (341)**

Using the reverse set up of example 2 with a HIGH at U9-3, U9-6, U4-3, U4-6 and U3-15 and a LOW at U9-2, U9-7, U4-2 and U4-7. The decimal equivalent would be 341. This would result in an initial configuration of HIGH at Pad LL, LOW at U5-10, HIGH at U6-10, LOW at U6-11, HIGH at U2-10, LOW at U2-11, HIGH at U2-12, LOW at U2-13 and HIGH at U2-14. Again only U2 has all of its inputs so that they can be decoded. The result from the Truth Table would be a HIGH at

U2-1/U6-12 and a LOW at U2-2/U6-13 and U2-3/U6-14. It also provides a LOW at U2-4/U1-12 and U2-5/U1-13 and a HIGH at U2-6/U1-14. U6 can now be decoded for a HIGH at U6-4/U1-10 and a LOW at U6-1/U5-11, U6-2/U5-12, U6-3/U5-13 and U6-5/U1-11. All of the inputs to U5 are LOW and this decodes to all outputs LOW at Pads KK, JJ, HH and RR. There are HIGH inputs to U1 at pins 10 and 14 and this decodes to a LOW at U1-1/Pad PP, HIGH at U1-2/Pad NN, LOW at U1-3/Pad MM, HIGH at U1-4/Pad 33, HIGH at U1-5/Pad 34 and LOW at U1-6/Pad 35. The final result is a HIGH at Pad LL and a LOW at Pads KK, JJ and HH. These will be decoded on the Display Panel to display a One. Pads RR, PP and MM will be LOW and Pad NN HIGH. This will decode on the Display Panel to display a Four. Pads 33 and 34 will be HIGH and Pad 35 LOW. This will decode in the Display Panel a display to Three. Display will be the decimal number 341.

3.19 RAM BUFFER (201-24137)

The RAM Buffer assembly contains the 4096 Bit memory and its associated Read, Write and Addressing circuitry.

The memory is laid out in two sections, each containing eight 256 x 1 RAM's. One section is used for the 256 LOW order bits and the other for the 256 HIGH order bits to obtain up to 512 eight-bit words.

3.19.1 Addressing

The eight LOW order Address bits (A_0–A_7) are input to the board on Pads 1-5 and A-C respectively. This HIGH for Data input is inverted and applied to both sections of the RAM simultaneously. The HIGH Order Address bit (A_8) is input on Pad D and applied directly to the left section and inverted at U22-3 and applied to the right section. In this manner only one section of the RAM's will be enabled at any one time even though both are addressed at the same time.

3.19.2 Data Input

The Data input is on Pads M-V for DI_1 through DI_8 respectively. The HIGH for data present will be inverted by U18 or U21 and applied to the input of the two RAM's associated with the data level. The HIGH order bit of the address will determine which of the two RAM's the data is written into with the arrival of a Write pulse.

3.19.3 Write

For the purpose of this discussion it is assumed that the RAM has been selected as the output and some other device has been selected as the input.

Selecting the RAM as the output will bring a LOW signal into the assembly on Pad PP from the Control Switch assembly. This LOW will enable U23-2. It will also be inverted at U23-13 and again at U21-10 for a LOW output at Pad 19 and at U21-12 for a LOW output at Pad W. The LOW output at these two pads will turn ON the "Data A" and "Data B" indicators on the Display Panel.

Selecting some other device leaves the RAM Input switch open and a HIGH is input at Pad RR from the Control Switch assembly. This input is inverted at U23-10 to apply a disabling LOW to U22-13.

The Write pulse will be input at Pad AA from the Control Card assembly as a HIGH to LOW going pulse. This will be sensed at U23-3 and the resulting HIGH pulse will strobe the Write input to all 16 RAM's.

The Output gates will also be enabled at all times except with the LOW to HIGH going Read pulse (Pad X) and Address pulse (Pad 24). This is to enable both the "Input" and "Output" display lights on the Display Panel for the operators convenience.

3.19.4 Read

For the purpose of this discussion it is assumed that the RAM has been selected as the input and some other device has been selected as the output.

Selecting the RAM as an input will bring in a LOW signal on Pad RR from the Control Switch assembly. This LOW will be inverted at U23-10 and applied to U22-13 as a HIGH enabling signal. Since the RAM is not selected as the output, Pad PP will be HIGH disabling U23-2 and a HIGH will be supplied to the "Data A" and "Data B" lights.

With the arrival of the LOW to HIGH Read pulse at Pad X from the Control card, U22-11 will go LOW and U22-8 HIGH to strobe the Output gates U19 and U20. The resulting LOW for data present will be output on Pads 11 through 18 for levels DO_1 through DO_8 respectively to the selected Output device.

3.19.5 Read and Write

For the purpose of this discussion it is assumed that the RAM has been selected as both Input and Output device. This condition usually occurs when used in conjunction with the keyboard to correct or change data in the RAM.

With the RAM selected for both input and output, both Pads PP and RR will be LOW from the Control Switch assembly. The LOW at RR will be inverted by U23-10 and will enable U22-13. The LOW at PP will enable U23-2, be inverted at U23-13 to enable U22-4 and be inverted again at U21-10 and U21-12 to turn ON the "Data A" and "Data B" lights.

The Output gates will be enabled at all times except when an Address pulse is present from the Control card.

Data will be written into the RAM's only with a Write pulse from the Control card.

3.20 PERF DRIVER (201-24521)

The Perf Driver board contains the Timing circuits and drivers required to interface to the Perforator.

3.20.1 Code Perforation

All codes to be perforated are input to this board through Pads D-M for levels 1-8, respectively. The code levels input will be in the form of pulses from HIGH to LOW. This will result in the Q output of the affected latch going LOW and the $\overline{Q}$ output going HIGH. With the Perforator selected as an output, Pad V will be LOW from the Control Switch assembly and U9-2 will be enabled. The next Write pulse on Pad T from the Control card will lock the code into the buffer and supply a LOW input to U9-3 for a HIGH output at U9-1. This will be AND gated with the HIGH at U18-10 to provide a LOW through the U10 drivers. U10-3 will continue to lock the code into the buffer until the Reverse Perf Timing pulse clears the circuitry. U10-5 supplies the LOW to Pad S as a Perf Busy which will inhibit the Control Card Timing circuits. The LOW from U18-8 also is applied to U14-5 to provide a HIGH to U15-1. This

indicates that a character is locked in the buffer and must be perforated. U15-2 will be supplied with a HIGH by the Reverse Timing circuit at the time the Forward (positive) Timing pulse is input through Pad Y.

When the Positive Timing pulse is input through Pad Y, Q3 will conduct and supply a LOW to the U15-17 Reverse latch and the U15/U14 Forward latch. The LOW input to U14-10 will set the Forward latch LOW at U15-12. This LOW is inverted by U11-1 and 2 to provide a HIGH condition at Pad R as a DS signal (Data Strobe). The Data Strobe is not used in this configuration. The LOW condition at U15-12 also is inverted through U11-5 and 6 and provides a HIGH to U13-10. This HIGH is AND gated with a HIGH at U13-9 to produce a LOW at U13-8 which is output through a U16 driver to Pad W as a Forward Magnet command and to Pad 12 as $\overline{DS}$ (Data Strobe Inverted). The $\overline{DS}$ is not used in this configuration. The U13-8 LOW condition is inverted and provides a HIGH to U13-12 and 13 to produce a LOW at U13-11. The LOW condition at U13-11 is inverted and provides a HIGH to U13-6 for strobing the output Data gates and is output to the Perf through a U16 driver and Pad Z as the Sprocket Magnet command.

The previously described conditions will exist until the Negative Timing pulse is input through Pad Y. At that time, Q2 will turn OFF and cause U11-10 to output a LOW pulse which is supplied to U17-12 (Reverse latch) as a Set input and U15-2 as a Reset signal. U15-12 will be reset HIGH which will terminate all the outputs described when it was set LOW. Additionally, U17-8 will go LOW which will cause U12-4 to output a LOW to U18-10 and remove the lockup from the buffer.

The output of the Data gates is supplied through two paths. One is through the drivers and Pads 15-22 to the Perforator. The other is from the output of the gate itself through Pads 4-11. This output is not used in this configuration.

3.20.2 Turn-On Conditioner

The circuit comprised of Q1 and its associated components form a Turn-On conditioner. This insures that there will be no outputs from the Perf Driver board to the Perforator at the time power is applied.

3.20.3 6-Level/8-Level

On the Perf Driver board a jumper plug is provided for selecting a 6-level output or an 8-level output. When in the 6-level position, the jumper plug supplies a LOW condition to the level 7 and 8 Output gates thereby disabling them. In the 8-level position the jumper plug connects the Data Strobe to the level 7 and 8 Output gates so they will be strobed in the same manner as the gates for levels 1-6.

3.20.4 Forward Feed, Reverse Feed and Perf Inhibit Inputs

These inputs on Pads N, P and U respectively and their associated circuitry are not used in this configuration. The inputs should always remain at a HIGH level.

3.21 INTERFACE ASSEMBLIES (201-24214 and 201-24543)

These two assemblies are identical except the number of pins connected. Interface assembly, Dual 16 pin (201-24214) contains two 16 pin dip sockets while the Interface assembly Dual 24 pin (201-24543) contains the 24 pin dip sockets.

The left socket is normally connected to the Program or Read Only card installed in the MEU connector labeled PROM 1 (J3-M) while the right socket normally connects to the card installed in the connector labeled PROM 2 (J4-M).

Care must be taken that the Program and/or Read Only cards and Interface assembly are compatible with the ROM to be programmed.

One Interface assembly comes as an integral part of the Programmer. Either one may be selected. The other is available as an option if desired.

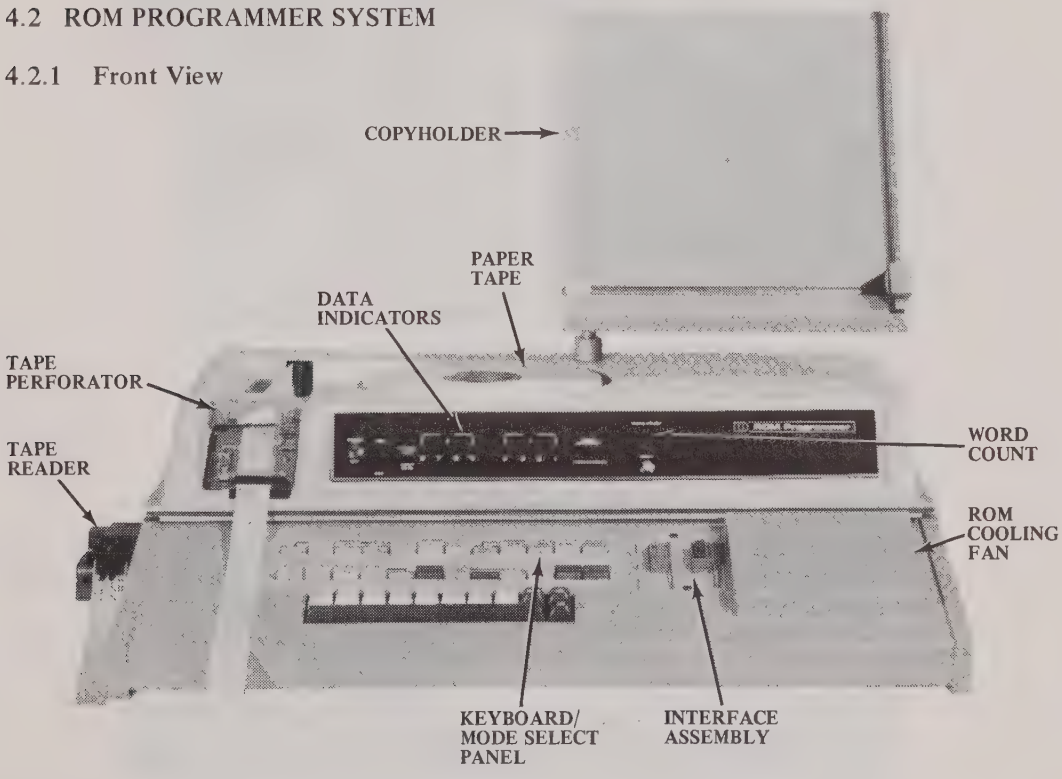
SECTION 4
CIRCUIT BOARD LAYOUT AND PARTS LIST

4.1 GENERAL

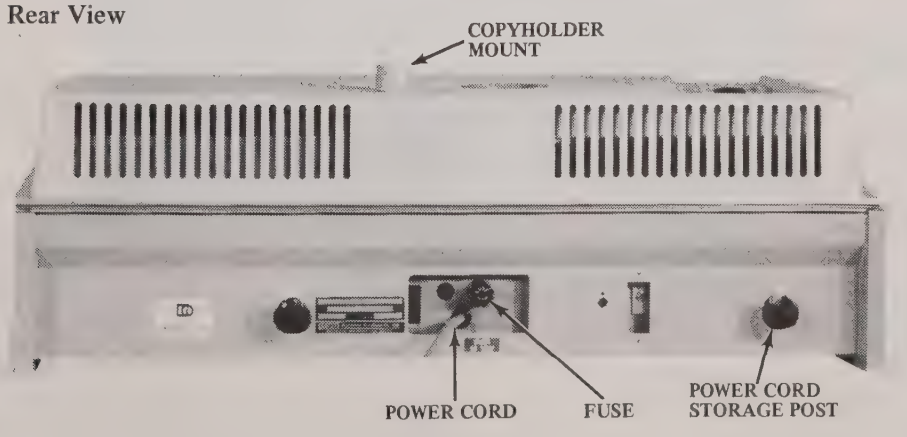
Provided in this section of the manual are photos and diagrams showing the physical layout of the system. These layouts will aid the technician in locating sub-assemblies and components within the system.

4.2 ROM PROGRAMMER SYSTEM

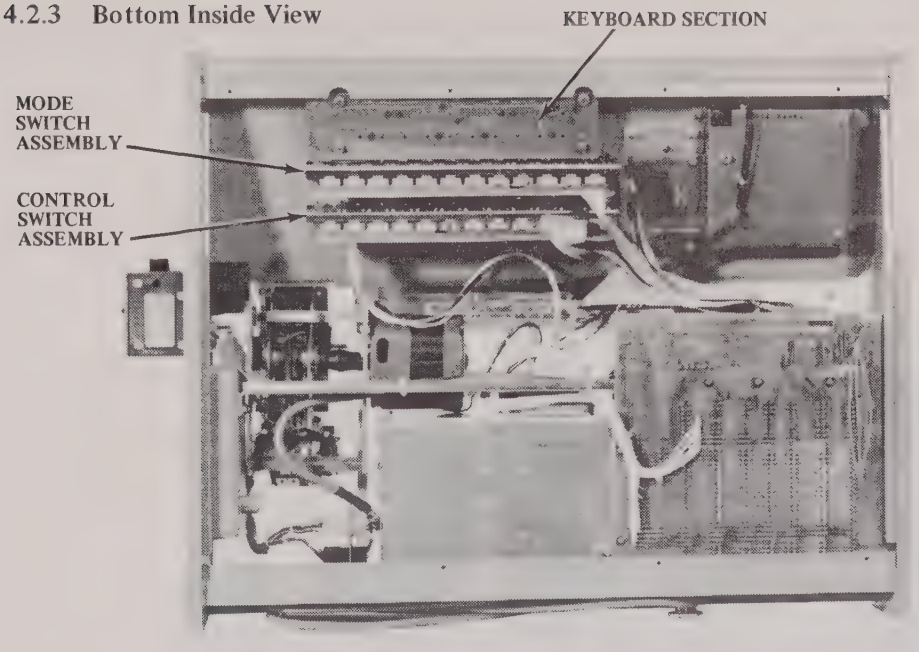
4.2.1 Front View



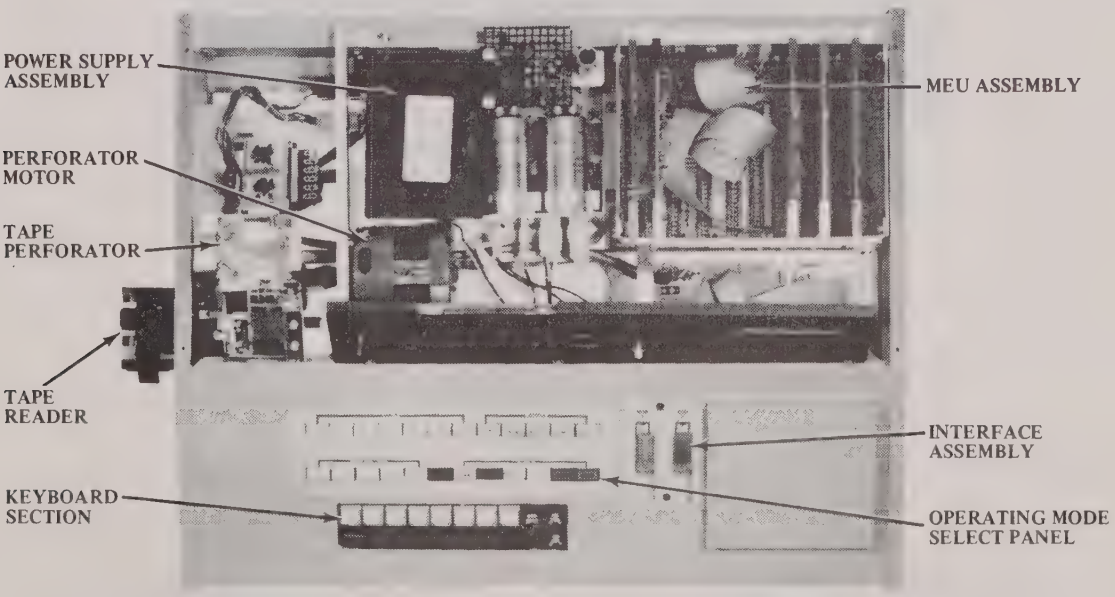
4.2.2 Rear View



4.2.3 Bottom Inside View



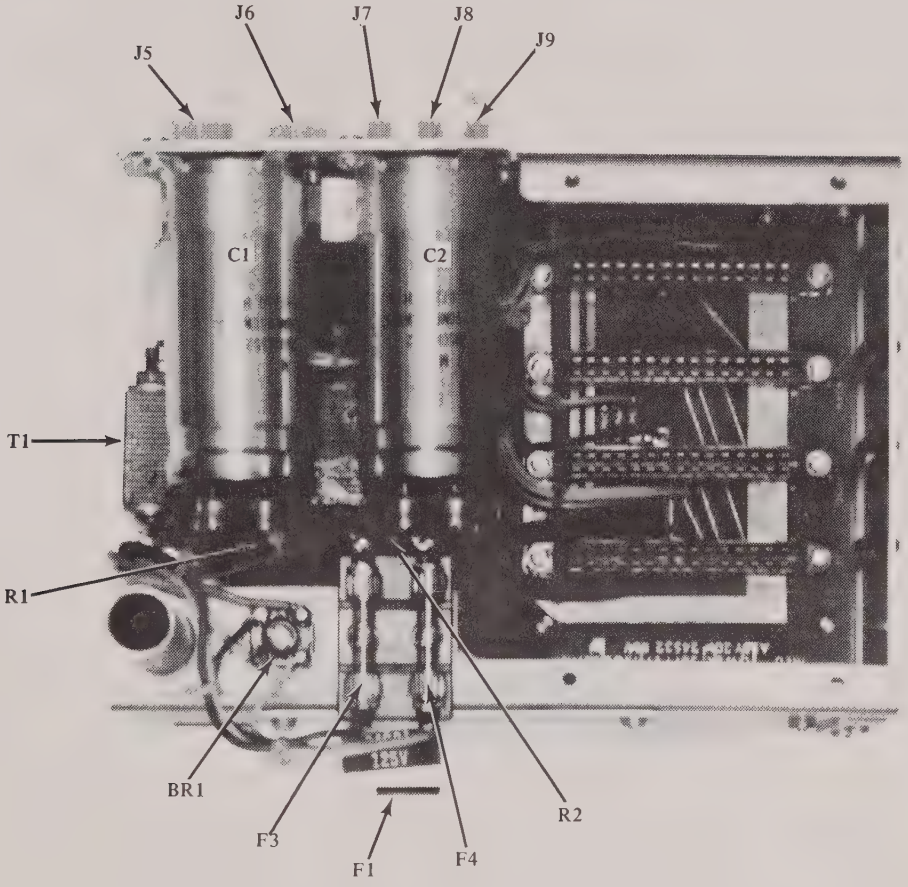
4.2.4 Top Inside View



DESCRIPTION	PART NUMBER
READER CTR FEED	104-25548
PERF DRIVE ASSY CF	211-26034
PERFORATOR HEAD - CF - 8 LEVEL	304-20816
MOTOR 1/40 HP CCW 115V	424-22444
COUPLING FLEX 3/16 X 5/16	506-20813
TUBE CHAD	514-23287
INTERFACE ASSEMBLY 16 PIN	211-24128
INTERFACE ASSEMBLY 24 PIN	211-24542

DESCRIPTION	PART NUMBER
ENCLOSURE ASSY	208-24121
BASEPLATE ASSY	211-24513
FAN	424-20472
FAN ASSY	211-24839
SPARE PARTS KIT	490-25529
CHAD BOX ASSY	204-24290
COPYHOLDER ASSY	211-21899

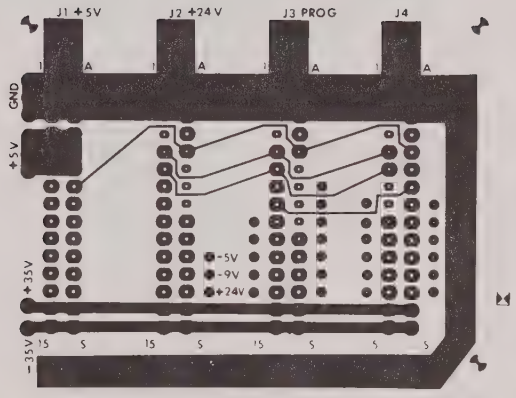
4.2.5 Power Supply Assembly (203-24125)



DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
BR1	KBPC02 BRIDGE RECTIFIER	450-22397	–	BLOCK - DUAL 3AG TYPE	422-22514
R1-2	5.1K 2W 5%	430-23218	T1	TRANSFORMER, POWER	485-24334
C1-2	3.5K MFD 50V	405-22396	J5	CONN. 12 PIN F	420-21732
F1	2 AMP 125V SLO-BLO	422-22638	J6	CONN. 6 PIN F	420-20619
F3-4	2 AMP 250V 3AG	422-27517	J7-9	CONN. 3 PIN F	420-20501
–	HOLDER	422-20432		MEU PWR. SUP ASSY	201-24532

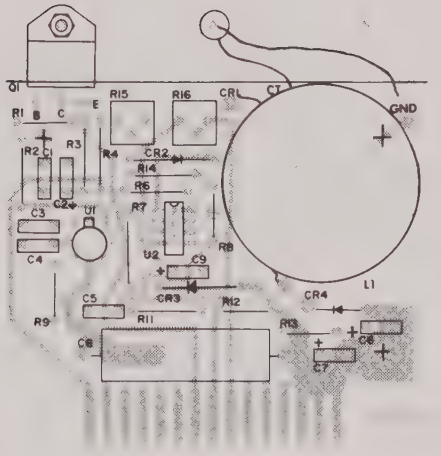
4.3 ROM PROGRAMMER CIRCUIT BOARDS

4.3.1 MEU Power Supply Assembly (201-24532)



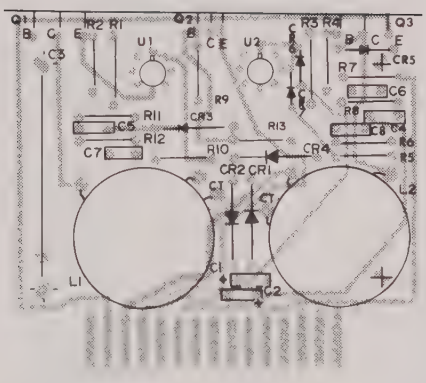
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
J1-4	CONNECTOR 15 PIN DUAL	420-24509	–	MEU POWER SUPPLY PWB	421-24533

4.3.2 +5 Volt Power Supply Assembly (201-24528)



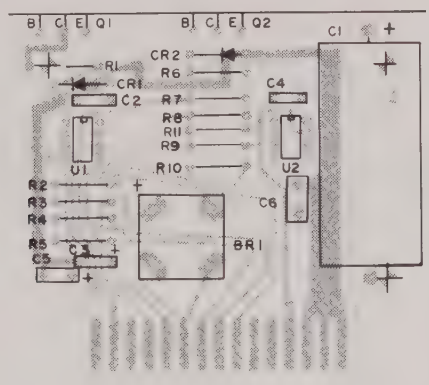
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1	TO5	470-24350	R9	16K 1/4W 5%	430-20131
U2	555SE TIMER	470-24361	R11	39K 1/4W 10%	430-20140
CR1	20 AMP, FAST RECOVER	450-23750	R13	3.9K 1/4W 10%	430-20116
			R14	1.62K 1/8W 1%	433-24663
CR2-3	1N4735 6.2V ZENER	450-25951	R15-16	POTENTIOMETER 1 TURN 1K	434-24076
CR4	UZ8707 7.5V ZENER	450-22383	C1	.01MFD	401-20522
			C2, 9	1MFD	405-24358
Q1	TIP147C	440-24348	C3	.001MFD	401-20548
R1	180 1/4W 10%	430-20084	C4-5	.01MFD	401-20642
R2	2K 1/2W 5%	430-20276	C6-7	220MFD	405-22655
R3, 12	2K 1/4W 5%	430-20109	C8	4MFD	404-22723
R4, 7	3K 1/2W 5%	430-20280	L1	CENTER TAP 12 AMP	485-23770
R6	3.01K 1/8W 1%	433-24662		+5 PWR SUPPLY PWB	421-24529
R8	270 1/4W 10%	430-20088			

4.3.3 +24 Volt Power Supply Assembly (201-24526)



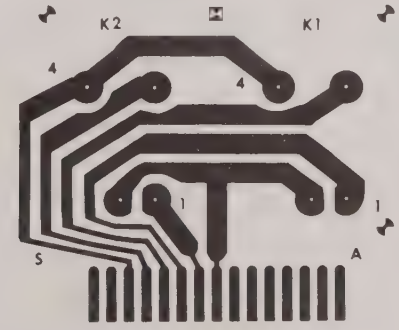
DESIGNATION	DESCRIPTION	PART NUMBER
U1-2	TO5	470-24350
CR1-2, 5	1N5186 100V	450-22407
CR3	1N751A 5.1V ZENER	450-22381
CR4	1N4742/UZ8712 12V ZENER	450-24352
CR6-7	1N4148	450-20511
Q1	TIP142C	440-24349
Q2	TIP32A	440-22387
Q3	TIP147C	440-24348
R1, 3	2K 1/2W 5%	430-20276
R2, 4	180 1/4W 10%	430-20084
R5	20K 1/4W 1%	433-22419
R6, 10	4.99K 1/8W 1%	433-24580
R7, 11	39K 1/4W 10%	430-20140
R8, 12	5.1K 1/4W 5%	430-20119
R9	4.02K 1/8W 1%	433-24581
R13	150 1/4W 10%	430-20082
C1	47MFD 35VDC	405-22653
C2	100MFD 20VDC	405-22656
C3	4MFD 100V	404-22723
C4-7	.01MFD 50VDC	401-20642
C8	.001MFD 50V	408-21864
L1-2	30 AMP, CENTER TAPPED	485-24360
	+24 PWR. SUPPLY PWB	421-24527

4.3.4 Programmable Power Supply Assembly (201-24530)



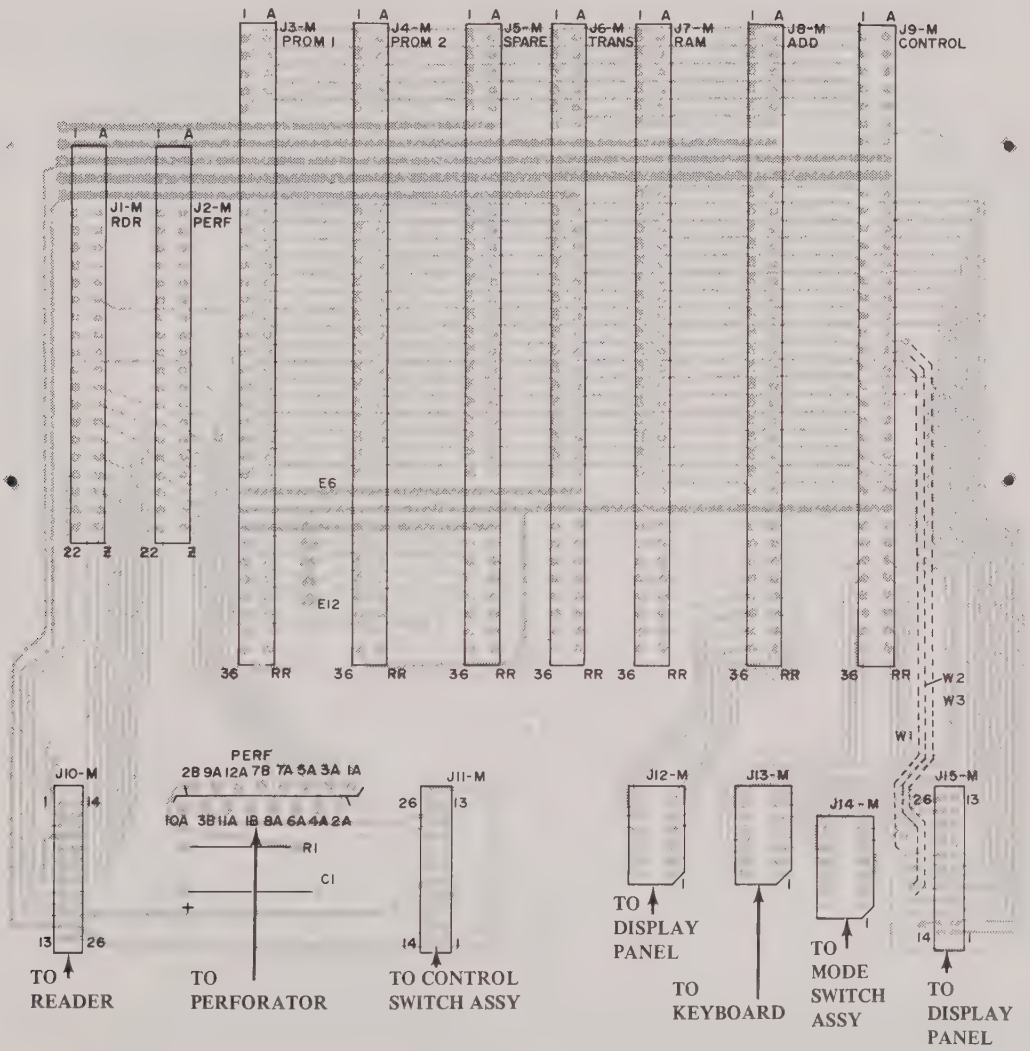
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1-2	U9T7741393	470-22342	R7	3.9K 1/4W 10%	430-20116
BR1	200V 5 AMP		R8	12.1K 1/4W 1%	433-21695
	BRIDGE		R9	10.5K 1/4W 1%	433-22408
	RECTIFIER	450-26136	R10	17.4K 1/8W 1%	433-24357
CR1	1N751A 5.1V	450-22381	R11	22K 1/4W 10%	430-20134
CR2	1N4148	450-20511	C1	500MFD 75V	405-24578
Q1, 2	TIP142C	440-24349	C2	.01MFD 50VDC	401-20642
R1	8.2K 1/2W 10%	430-20291	C3	.1MFD 35V	405-23655
R2	6.04K 1/8W 1%	433-24579	C4	.001MFD 1000V	401-20548
R3	4.99K 1/8W 1%	433-24580	C5	47MFD 35VDC	405-22653
R4	11K 1/8W 1%	433-24355	C6	100PFD 1KV	401-25014
R5	39K 1/4W 10%	430-20140		PROG PWR.	
R6	1K 1/4W 10%	430-20102		SUP PWB	421-24531

4.3.5 AC Motor Control Assembly (201-24607)



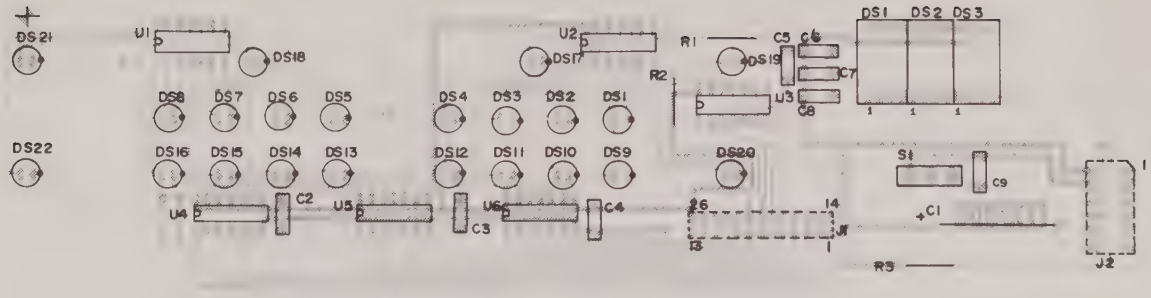
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
K1-2	RELAY 1½ AMP			AC MOTOR	
	PCB CTL	425-24612		CTL PWB	421-24608

4.3.6 MEU Connector Assembly (201-24093/201-24927)



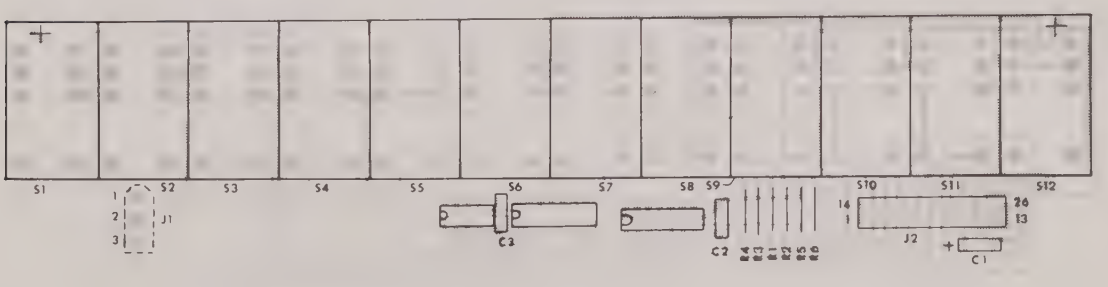
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
–	MEU CONN. ASSY (PROG I)	201-24093	–	MEU/POWER CABLE	210-24840
–	MEU CONN. ASSY (PROG II)	201-24927	J1-2	CONN. DUAL 22 PIN	420-20532
R1	68 2W 10%	430-20377	J3-9	CONN. DUAL 36 PIN	420-24206
C1	47MFD 35VDC	405-20654	J10-11, 15	PIN SQ. POST	486-23413
–	CABLE ASSY MEU PERF (PROG I)	210-22210	J12-14	DIP CONN. ASSY 16 PIN	211-23478
			–	MEU CONN. PWB	421-24094

4.3.7 Assembly Front Panel (201-23749)



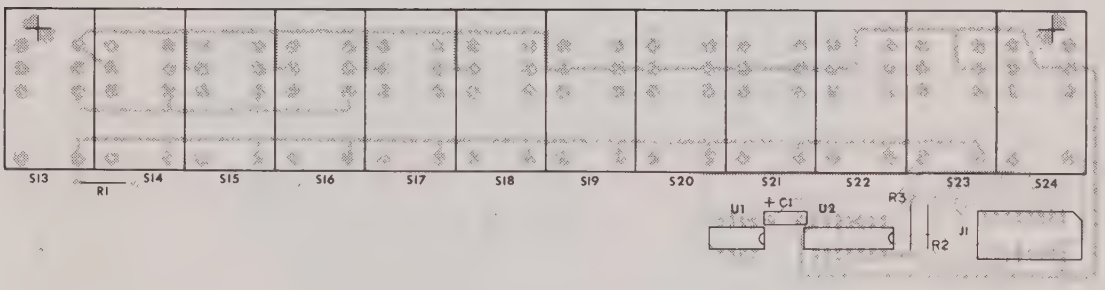
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1-2	13 DIP 220	430-23968	R1-3	1K 1/4W 10%	430-20102
U3	SN7406N	460-23018	C1	22MFD 15VDC	405-23879
U4-6	SN7407N	460-23974	C2-9	.01MFD 50VDC	401-20642
DS1-22	DISPLAY-RED RL-2 LED	475-21776	J2	DIP CONN. ASSY 16 PIN	211-23478
DS23-25	NUMERIC DISPLAY-VISUAL	423-24053	–	SOCKET DIP 24 PIN	420-23784
S1	SPDT SWITCH PUSHBUTTON	480-21775	–	PWB FRONT PANEL	421-23732

4.3.8 Control Switch Assembly (201-24129)



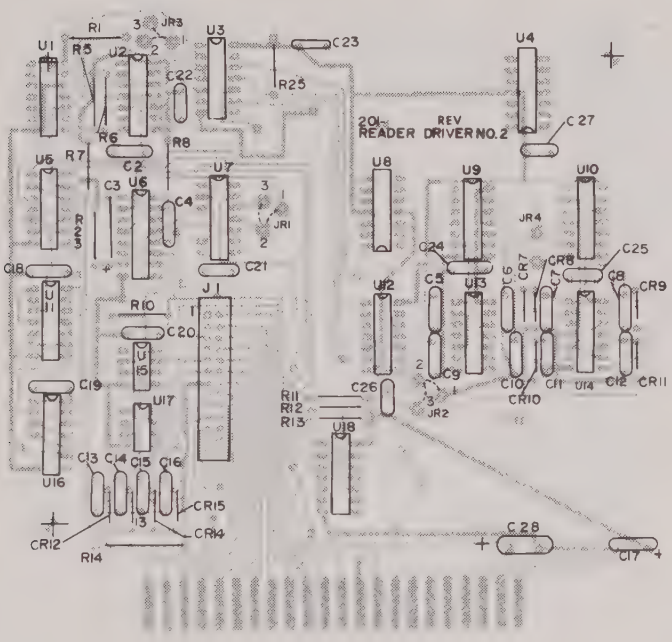
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1	SN75452N	460-23559	S1-12	SWITCH INTERLOCK	480-24646
U2	SN7404N	460-20414		LAMP 24V	423-24645
U3	SN7410N	460-20020		INSERT	423-24644
R1-6	1K 1/4W 10%	430-20102	–	CAP CLEAR	423-24639
C1	22MFD 15VDC	405-23879		CAP YELLOW	423-24641
C2, 3	.01MFD 50VDC	401-20642		CONTROL SWITCH PWB	421-24130
J1	CONN. 3 PIN F	420-20501			

4.3.9 Mode Switch Assembly (201-24545)



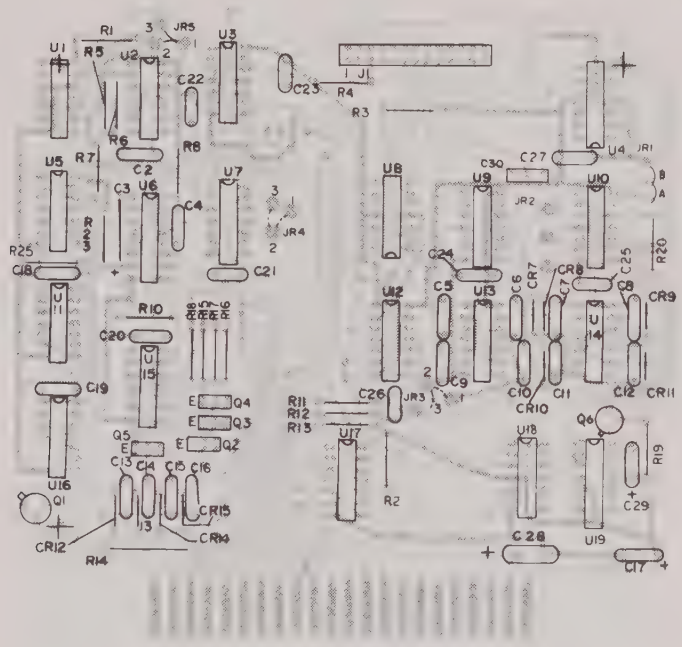
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1	SN74451P	470-20039	-	CAP RED	423-24640
U2	SN7400N	460-20412	-	CAP YELLOW	423-24641
R1-3	1K 1/4W 10%	430-20102	-	CAP GREEN	423-24642
C1	1MFD	405-24358	-	CABLE ASSY	
S13-24	SWITCH INTLK	480-24647		16 PIN M	
	LAMP 24V	423-24645		13 INCH	210-23852
	INSERT	423-24644		MODE SWITCH	
-	CAP CLEAR	423-24639		PWB	421-24546

4.3.10 Addmaster Reader/Driver 2 Assembly (201-24569)



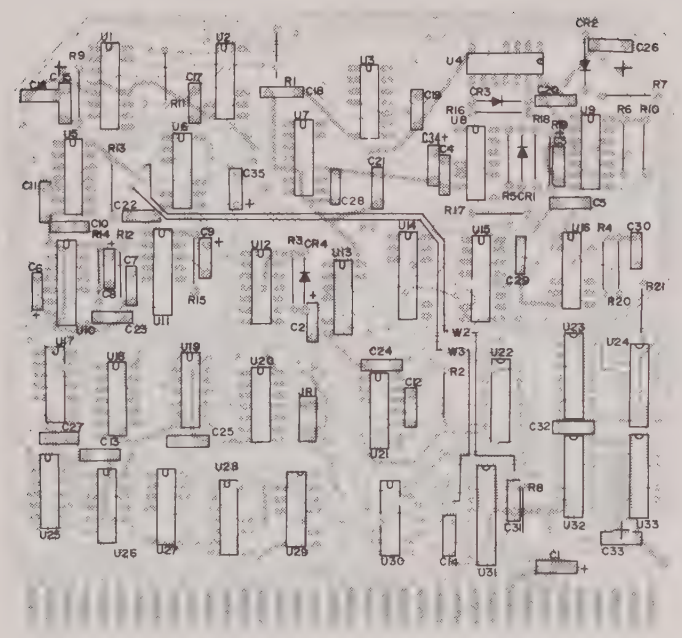
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1-2, 16	DM8510N	460-20019	R7, 10-13	2.2K 1/4W 10%	430-20110
U3	SN7410N	460-20020	R8	20K 1/4W 5%	430-20133
U4, 8	MC9818P	462-23989	R14	430 1W 5%	430-20342
U5	SN7400N	460-20412	R23	39K 1/4W 10%	430-20140
U6	SN74123N	460-23025	C2, 4-16, 18-27	.01MFD 50VDC	401-20642
U7	SN7402N	460-20411	C3	1MFD 50VDC	405-20523
U9-10, 18	DM936N	461-20030	C17	22MFD 15VDC	405-23879
U11, 13-14	DM946N	461-20032	C28	47MFD 35VDC	405-22653
U12	DM930N	461-22245	S1-4	PLUG-SHORTING	
U15, 17	SN75452N	460-23559		.040 PINS	420-21725
CR7-15	1N4148	450-20511		ADDM RDR/	
R1, 5, 25	1K 1/4W 10%	430-20102		DR NO. 2	
R6	2K 1/4W 5%	430-20109		PWB	421-24570

4.3.11 Addmaster Reader/Driver 3 Assembly (201-26963



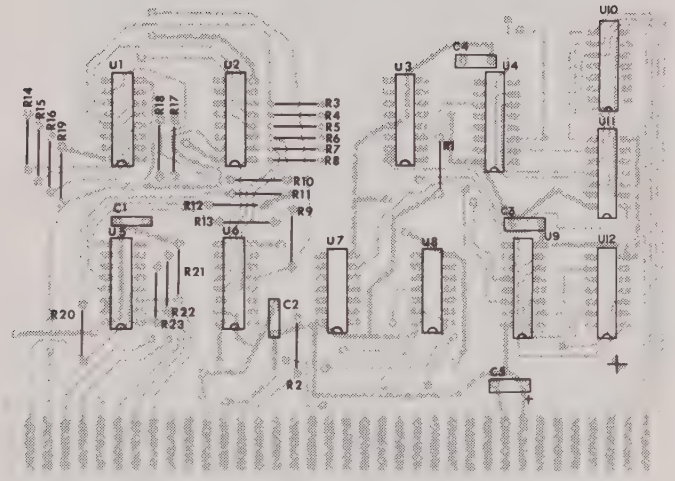
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1-2, 16, 18	DM8510N	460-20019	R2-3, 7, 10-13, 20	2.2K 1/4W 10%	430-20110
U3	SN7410N	460-20020	R6	2K 1/4W 5%	430-20109
U4, 8	MC9818P	462-23989	R8	20K 1/4W 5%	430-20133
U5	SN7400N	460-20412	R14	430 1W 5%	430-20342
U6	SN74123	460-23025	R15-18	470 1/4W 10%	430-20094
U7	SN7402N	460-20411	R19, 23	39K 1/4W 10%	430-20140
U9-10, 17	DM936N	461-20030	C2, 4-16, 18-27	.01MFD 50VDC	401-20642
U11	SN7486N	460-21772	C3	1MFD 50VDC	405-20523
U12	DM930N	461-22245	C17, 28	4.7MFD 10V	405-23515
U13-14	DM946N	461-20032	C29	10MFD 20V	405-23517
U15	SN7408N	460-22913	C30	.1MFD 100VDC	401-21923
U19	DM8533N	460-20027	JR2-5	PLUG-SHORTING	420-21725
Q1, 6	2N2222 NPN	440-20518	J1	PIN-SQUARE POST	486-23413
Q2-5	MJE800	440-26810		ADDM RDR/ DVR 3 PWB	421-26964
CR7-15	1N4148	450-20511			
R1, 4-5, 25	1K 1/4W 10%	430-20102			

4.3.12 Control Card Assembly (201-24810)



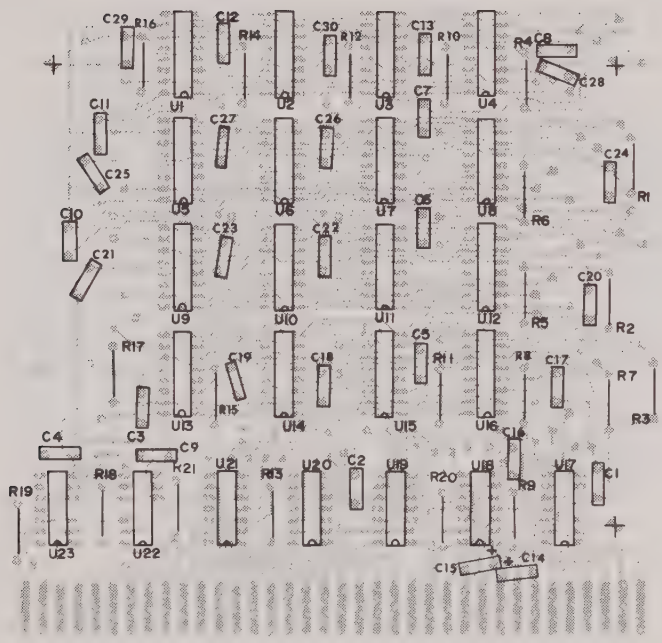
DESIGNATION	DESCRIPTION	PART NUMBER
U1, 15, 31	SN7476N	460-20022
U2, 9, 21	SN7402N	460-20411
U3, 17-18, 26-27	DM8510N	460-20019
U4	SN7404N	460-20414
U5, 13	SN7400N	460-20412
U6	SN7410N	460-20020
U7	DM8533N	460-20027
U8	SN7413N	460-22909
U10-11	SN74123N	460-23025
U12	SN7425N	460-23019
U14	SN7442N	460-20026
U16	SN7403N	460-21788
U19-20, 23, 28-29	SN7486N	460-21772
U22	SN7409N	460-22920
U24	SN7430N	460-20034
U25, 30	13 DIP 1K	430-23582
U32-33	SN7405N	460-22324
CR1-4	1N4148	450-20511
R1, 4-11, 18, 20-21	1K 1/4W 10%	430-20102
R2	2.2K 1/4W 10%	430-20110
R3, 12, 16	10K 1/4W 10%	430-20126
R13	47K 1/4W 10%	430-20142
R14	22K 1/4W 10%	430-20134
R15	15K 1/4W 10%	430-20130
R17	100 1/4W 10%	430-20078
R19	270 1/4W 10%	430-20088
C1	22MFD 15VDC	405-23879
C2, 9	10MFD 20V	405-23517
C3	.1MFD 100VDC	401-21923
C4, 6, 35	.1MFD 35V	405-23655
C5, 10-34	.01MFD 50VDC	401-20642
C7	.002MFD 500V	401-25272
C8	47MFD 35VDC	405-22653
JR1	PLUG-SHORTING .040 PINS	420-21725
	PWB CONTROL CARD	421-24811

4.3.13 Address Card Assembly (201-24133



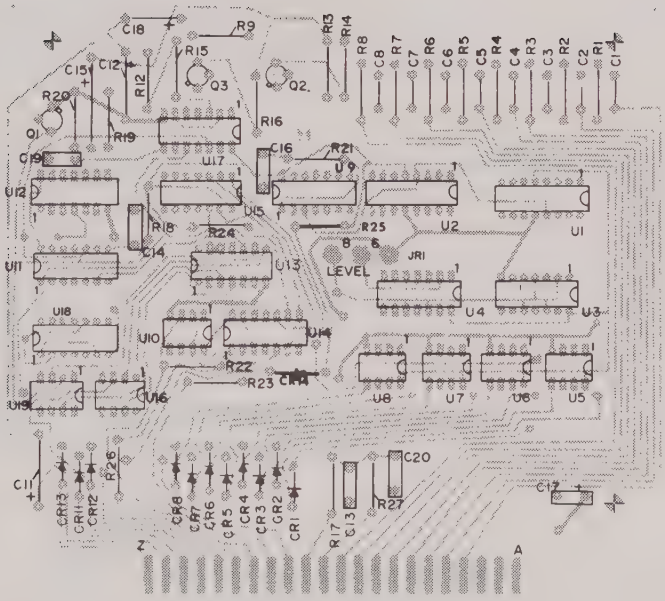
DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1-2, 5-6	SN74185N	460-23112	U11-12	SN7407N	460-23974
U3	SN7476N	460-20022	R1-23	1K 1/4W 10%	430-20102
U4, 9	SN74193N	460-21773	C1-4	.01MFD 50VDC	401-20642
U7	SN7404N	460-20414	C5	22MFD 15VDC	405-23879
U8	SN7400N	460-20412		ADDRESS CARD	
U10	13 DIP 1K	430-23582		PWB	421-24134

4.3.14 RAM Buffer Assembly (201-24137)



DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1-16	MM2501 256 X 1 RAM	465-22562	U23	SN7402N	460-20411
U17-18	SN7404N	460-20414	R1-21	1K 1/4W 10%	430-20102
U19-20	SN7403N	460-21788	C1-13, 16-30	.01MFD 50VDC	401-20642
U21	SN7405N	460-22324	C14-15	22MFD 15VDC	405-23879
U22	SN7400N	460-20412		RAM BUFFER PWB	421-24138

4.3.15 Perf Driver Assembly (201-24521)



DESIGNATION	DESCRIPTION	PART NUMBER	DESIGNATION	DESCRIPTION	PART NUMBER
U1-2	SN7475N	460-20410	R20	100K 1/4W 10%	430-20150
U3-4, 13-14, 17-18	SN7400N	460-20412	R21	100 1/4W 10%	430-20078
U5-8, 10, 16, 19	SN75451P	470-20039	C1-8, 13-14, 19-20	.001MFD 50V	408-21864
U9	SN7402N	460-20411	C11, 18	2.2MFD 35VDC	405-20638
U11	SN7404	460-20414	C12	.1MFD 50VDC	405-20641
U12	DM935N	461-20037	C15	4.7MFD 35VDC	405-21248
U15	SN7410N	460-20020	C16	.01MFD 50VDC	401-20642
CR1-8, 11-14	1N4148	450-20511	C17	22MFD 15VDC	405-23879
Q1-3	2N2222 NPN	440-20518	–	PLUG-SHORTING .040 PINS	420-21725
R1-8, 14, 16-18, 22-27	2.2K 1/4W 10%	430-20110		PERF DRIVER PWB	421-24522
R9, 12-13, 15	10K 1/4W 10%	430-20126			
R19	47K 1/4W 10%	430-20142			

SECTION 5
SYSTEM INSTALLATION AND CHECK-OUT PROCEDURE

5.1 GENERAL

The packaging of equipment at DATA I/O is done carefully and thoroughly. However, there is always the possibility of damage to the system due to rough handling in transit. Therefore, when a system is received it should be unpacked and inspected thoroughly for any possible damage.

If the installation and check-out is to be performed by operator level personnel, a technician should be summoned at the first indication of a problem to minimize the possibility of damage to electronic components.

5.2 POWER

The ROM Programmer is available in units for operation on either 110 volts, 60 Hz or 220 volts, 50 Hz. Insure that the machine delivered matches the local line voltage before applying power to the Programmer.

Both types should be provided with a separate 3-wire AC power line to insure minimum line voltage variations and prevent voltage spikes from occurring due to other heavy electrical loads.

5.3 FUNCTIONAL CHECK-OUT

The test described in the following paragraphs will insure that the Programmer standard circuits and functions are operating correctly.

If checking a Programmer II without the Perforator, omit paragraph 5.3.6.

NOTE: The ENTRY BAR, ADD FWD and ADD REV keys are of the cyclic type. If they are not released within one quarter of a second, the action will be repeated at a rate of 10 characters per second until the key is released.

5.3.1 Indicator Check

Select KEYBD on the Input section.

Select RAM in the Output section.

Select 512 Data Length.

Select INSERT and MANUAL on the Mode section.

NOTE: A Program card should be installed if available.

Turn the POWER switch ON.

The "Power Interrupt" indicator should be ON.

The "Data A" and "Data B" indicators should be OFF.

All other indications are random.

Depress RESET to reset the "Word Count" to zero.

Depress START. The "Power Interrupt" indicator should be extinguished. The "FWD" indicator should come ON if it had not been ON.

Depress and hold the ADD FWD key. The "Word Count" should increase to 001 and after a short pause (approximately ¼ second) should continue to count at a rate of approximately ten counts per second.

Release the ADD FWD key in 3 to 5 seconds. The Word counter stops counting.

Depress and hold the ADD REV key. The "FWD" indicator goes out and the "REV" indicator comes ON. The "Word Count" decreases one count and after ¼ second rapidly decreases to zero.

Release the ADD REV key when the "Word Count" reaches 000. The "REV" indicator goes OUT and the "FWD" indicator comes ON.

Depress and hold the ADD FWD key. No indications change.

Release the ADD FWD key after at least ½ second. The "Word Count" advances to 001.

Select VERIFY on the Mode section. The "Data A" and "Data B" indicators should come ON. Select PROG on the Mode section. The "Data A" and "Data B" indicators should stay ON.

Depress RESET to reset the "Word Count" to zero.

Select AUTO on the Mode section.

Depress START. The "Word Count" advances to count 511.

Depress STOP then START. The "Word Count" should return to the count 000. This has cleared the RAM of random data.

Select KEYBD and RAM on the Input section.

Select MANUAL on the Mode section.

Depress STOP then START.

Depress BIT 1 through BIT 8 keys. All eight "Input Data" indicators should come ON.

Depress WORD CLEAR. All eight "Input Data" indicators should go OUT.

Depress STOP then START. The "Word Count" should advance to the count 001.

Depress BIT 1 through BIT 8 keys. The eight "Input Data" indicators should come ON.

Momentarily depress the ENTRY BAR. The "Word Count" should advance to the count 002. See note in paragraph 5.3.

Momentarily depress the ADD REV key. The "Word Count" should decrease to the count 001 and all eight "Input Data" and all eight "Output Data" indicators should be ON.

Momentarily depress the ADD REV key. The "Word Count" should decrease to the count 000 and all eight "Input Data" and all eight "Output Data" indicators should be OFF.

5.3.2 **Verify Circuits**

Select KEYBD **only** on the Input section.

Select RAM in the Output section.

Select 32 Data Length.

Select PROG and MANUAL in the Mode section.

Depress RESET to reset the "Word Count" to zero.

Depress START, STOP, START.

At this time, the "Word Count" should be 001 and the "FWD" indicator should be ON.

Depress the BIT 1 key and then the ENTRY BAR. The "Word Count" should advance to 002.

Depress the BIT 2 key and then the ENTRY BAR. The "Word Count" should advance to 003.

Repeat for each BIT key until BIT key 8 has been entered into RAM at "Word Count" 008 and the "Word Count" indicator reads 009. Using the ENTRY BAR, advance the "Word Count" to at least a count of 012.

Momentarily depress the ADD REV key.

Select VERIFY in the Mode section. Depress the BIT 8 key followed by the ENTRY BAR. The "Word Count" should not change. Depress the WORD CLEAR key.

Repeat the check using each BIT key in turn followed by the ENTRY BAR and WORD CLEAR. This insures that the "Word Count" will not address if there is no verify.

Depress and hold the ENTRY BAR after clearing BIT 1 and the "Word Count" should decrease to the count of 008 and stop. "Output Data" indicator 8 should be ON.

Depress BIT 8 key followed by the ENTRY BAR. The circuit should verify and step to "Word Count" 007.

Repeat the step for each BIT key depressing the appropriate key for the "Word Count".

When the "Word Count" steps to 000, the check of the Verify circuit is complete.

5.3.3 Tape to Ram Step 1

Insert the Test Tape in the Tape Reader insuring that part of the blank leader is under the Read Head and the narrow portion of the tape, as divided by the Sprocket holes, is to the outside of the Tape Reader. Insure that the Tape Reader is turned ON by depressing the MOMENTARY ON switch to ON. The switch is located on the Tape Reader Head on the left side of the Programmer.

Depress RESET to set the "Word Count" to zero.

Select AUTO on the Mode section.

Depress START. The tape should advance entering data into RAM until the "Word Count" reaches 511.

Select VERIFY on the Mode section.

Depress STOP then START.

The tape should reverse through the Reader and verify that data on the tape and in RAM are identical.

5.3.4 Tape to Ram Step 2

Select PROG and MANUAL on the Mode section.

Depress STOP, START, STOP, START. The "Word Count" should advance to 001.

Depress RESET to set the "Word Count" to zero.

Select AUTO on the Mode section.

Depress START. The tape should advance entering data into RAM until the "Word Count" reaches 511.

Select VERIFY on the Mode section.

Depress STOP then START.

The tape should reverse through the Reader and verify that data on the tape and in RAM are identical.

5.3.5 Tape to Ram Step 3

Select PROG and MANUAL on the Mode section.

Depress STOP, START, STOP, START. The "Word Count" should advance to 001.

Depress RESET to set the "Word Count" to zero.

Select AUTO on the Mode section.

Depress START. The tape should advance entering data into RAM until the "Word Count" reaches 511.

Select VERIFY on the Mode section.

Depress STOP then START.

The tape should reverse through the Reader and verify that data on the tape and in RAM are identical.

5.3.6 Ram to Perforator

Select 64 Data Length.

Select PROG and MANUAL on the Mode section.

Depress STOP, START, STOP, START. "Word Count" should advance to 001.

Depress RESET to set the "Word Count" to zero.

Select AUTO on the Mode section.

Depress START. The tape should advance entering data into RAM until the "Word Count" reaches 63.

Select VERIFY on the Mode section.

Depress STOP then START.

The tape reverses through the Reader and verifies that the data on tape and in RAM are identical.

Select RAM on the Input section.

Select PERF on the Output section.

Select PROG on the Mode section.

Depress STOP then START.

Perforator advances and punches into tape the contents of the first 64 locations in RAM.

Select KEYBD on the Input section.

Depress STOP then START. Perforator advances blank tape.

Tear OFF tape from Perforator.

Remove Test Tape from Tape Reader.

Overlay two tapes insuring that the wide and narrow sections are together. Tape perforated should match the first 64 locations on the Test Tape.

5.3.7 Card Reader Check (Optional)

Prepare a card according to the Truth Table 5.1.

After the card is prepared, continue with the Functional Check of the Card Reader.

Turn the LINE POWER switch on the Mark Sense Card Reader to ON.

Insure that the POWER switch on the Tape Reader is ON.

Select KEYBD and RDR on the Input section.

Select RAM on the Output section.

Select 32 Data Length.

Select PROG and AUTO on the Mode section.

Depress RESET to set the "Word Count" to zero.

Depress START.

Insert the card into the Card Reader. The Card Reader will accept the card and feed it through the Reader. The "Word Count" will advance to count 31.

Depress RESET to set the "Word Count" to zero.

Depress VERIFY on the Mode section.

Depress START.

Insert the card into the Card Reader. The Card Reader will accept the card and feed it through the Reader. The "Word Count" will advance to count 31.

NOTE: If it stops on any other number, the VERIFY is not correct. Summon technical level personnel.

Depress RESET to set the "Word Count" to zero.

Select RAM on the Input section.

Select PERF on the Output section.

Select PROG and AUTO on the Mode section.

Depress START. The Perf advances and outputs a perforated tape. The "Word Count" advances to count 31.

Select KEYBD on the Input section.

Depress STOP then START.

The Perf advances and outputs a blank tape. The "Word Count" decreases to count 000.

Tear off the tape and verify that the punches correspond with the card prepared.

CARD TEST TRUTH TABLE
TABLE 5.1

Address	8	7	6	5	4	3	2	1
0	P	P	P	P	P	P	P	P
1	N	P	N	P	N	P	N	P
2	P	N	P	N	P	N	P	N
3	N	N	N	N	N	N	N	P
4	N	N	N	N	N	N	P	N
5	N	N	N	N	N	P	N	N
6	N	N	N	N	N	N	N	N
7	N	N	N	N	P	N	N	N
8	N	N	N	P	N	N	N	N
9	N	N	P	N	N	N	N	N
10	N	P	N	N	N	N	N	N
11	P	N	N	N	N	N	N	N
12	N	N	N	N	N	N	N	P
13	N	N	N	N	N	N	P	N
14	N	N	N	N	N	P	N	N
15	N	N	N	N	N	N	N	N
16	N	N	N	N	P	N	N	N
17	N	N	N	P	N	N	N	N
18	N	N	P	N	N	N	N	N
19	N	P	N	N	N	N	N	N
20	P	N	N	N	N	N	N	N
21	N	N	N	N	N	N	N	P
22	N	N	N	N	N	N	P	N
23	N	N	N	N	N	P	N	N
24	N	N	N	N	N	N	N	N
25	N	N	N	N	P	N	N	N
26	N	N	N	P	N	N	N	N
27	N	N	P	N	N	N	N	N
28	N	P	N	N	N	N	N	N
29	P	N	N	N	N	N	N	N
30	N	N	N	N	N	N	N	N
31	P	P	P	P	P	P	P	P

NOTE: The "P" stands for Program and will result in a punch in the tape. The "N" stands for Not Program and there will not be a punch in the tape at that location.

SECTION 6
MAINTENANCE

6.1 LUBRICATION

6.1.1 Perforator (Programmer I Only)

Periodically the Punch should be inspected. This inspection should determine whether the Punch needs lubrication or cleaning and lubrication. If cleaning is necessary, disassemble (as laid out in paragraph 6.4 and 6.5) and remove all dirt, paper, dust, lint and old lubricant using a lint free cloth and cleaning solvent if necessary. A non-toxic, non-flammable cleaning fluid should be used.

NOTE: Do NOT immerse the unit in cleaning solvents or ultra-sonic cleaners. Lubricate according to Table 6.1 and Figure 6.1.

6.1.2 Perforator Drive Motor (Programmer I Only)

The Perforator Drive motor requires one drop of light oil in each of the cups on the ends of the motor housing semi-annually.

6.1.3 Fan Motor

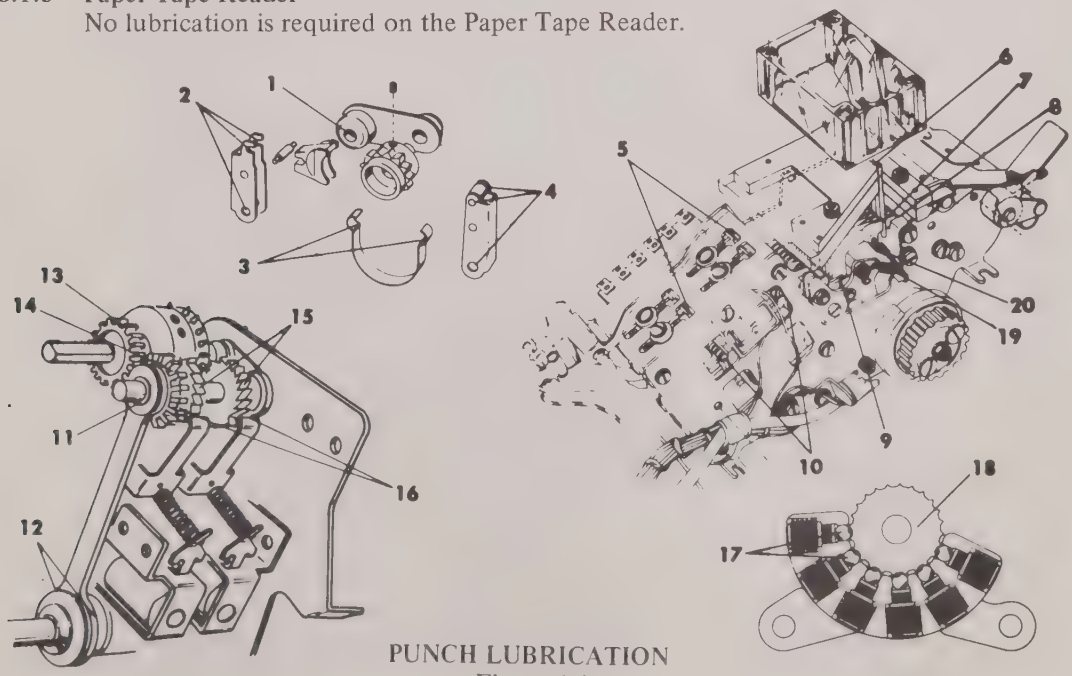
The Fan motor is a sealed unit and does not require any lubrication.

6.1.4 Rom Fan Motor

The Fan motor is a sealed unit and does not require any lubrication.

6.1.5 Paper Tape Reader

No lubrication is required on the Paper Tape Reader.



PUNCH LUBRICATION
Figure 6.1

PUNCH PREVENTATIVE MAINTENANCE LUBRICATION
TABLE 6.1

Fig. 6.1 Index No.	Name	Directions	Type of Lubricant
1	Ratchet Shaft Pivot Link	Inside hole and surface of Link	Custom Lube 700
2	Detent Arm Assembly	In four holes	Custom Lube 700
3	Detent Spring	As shown	Custom Lube 700
4	Detent Arm and Roll	Roll and Pivot Point	Custom Lube 700
5	Punch Magnet Armature Spring and Spacer	Both sides	Custom Lube 700
6	Punch Pin Guide Block	Very sparingly	Custom Lube 700
7	Punches	Top and bottom of slot	Custom Lube 700
8	Punch Driver Arm	Side of Arms	Custom Lube 700
9	Punch Pawl and Driver Arm Contact Points	All nine points	Custom Lube 700
10	Punch Magnet Armature Link Pivots	Lightly on all nine pivot points	Custom Lube 700
11	Index Link	Inside bearing surface, upper hole only	Custom Lube 700
12	Input Shaft Washer and Spacers	Both sides of Washers and Spacers	Custom Lube 700
13	Sprocket Gear	All teeth	Gulflex A
14	Ratchet Gear	All teeth	Gulflex A
15	Feed Ratchets	All teeth	Gulflex A
16	Index Magnet Interposers	Tip of Interposers	Gulflex A
17	Ball Detent Assembly	Grease packed within entire recess of housing	Gulflex A
18	Detent Wheel	All teeth	Gulflex A
19	Punch Pawl Yoke Spring Anchors	As shown	Gulflex A
20	Punch Pawl Spring Anchor Points	As shown	Gulflex A

6.2 PREVENTATIVE MAINTENANCE

6.2.1 Check List

When performing an inspection on the ROM Programmer the assemblies and associated parts listed must be throughly checked. Prior to performing an inspection refer to the Lubrication paragraph 6.1.

General
Remove all dirt and dust from the inner section of the Programmer. Replace any worn or broken parts. Insure that all circuit boards connectors are firmly in place.

Perforator (Programmer I Only)
Inspect for cleanliness. If lubrication required refer to paragraph 6.1.1.

Perforator Drive Motor (Programmer I Only)
Inspect shaft and coupling to Perforator for wear. Replace coupling as required. Inspect Drive motor for cleanliness.

If lubrication is required refer to paragraph 6.1.2.

Cooling Fan
Clean away loose dirt and debris. Fan is a replaceable sealed unit and no lubrication is required.

Rom Fan
Clean away loose dirt and debris. Clean filter screen. Fan motor is a replaceable sealed unit and no lubrication is required.

Paper Tape Reader
Clean away any loose dirt or debris. Reader motor is a sealed unit and no lubrication is required.

6.2.2 Machine Check Out

After completion of the inspection perform the Function Check-Out Procedures. (Refer to Section 5.3.) Correct any failures.

6.3 REGULATED POWER SUPPLY VOLTAGE AND ADJUSTMENT

NOTE: The regulated +5 and -9 voltage adjustments are made at the factory. Local readjustment could void the warranty. If an adjustment is made, it should be made only at the direction of Data I/O service personnel. The voltage should be rechecked after the Programmer has had approximately a 15 minute warm-up period. The Top Cover should be installed during this warm-up period to insure proper cooling. A voltmeter with an accuracy of at least 0.1 percent should be used when making any adjustment.

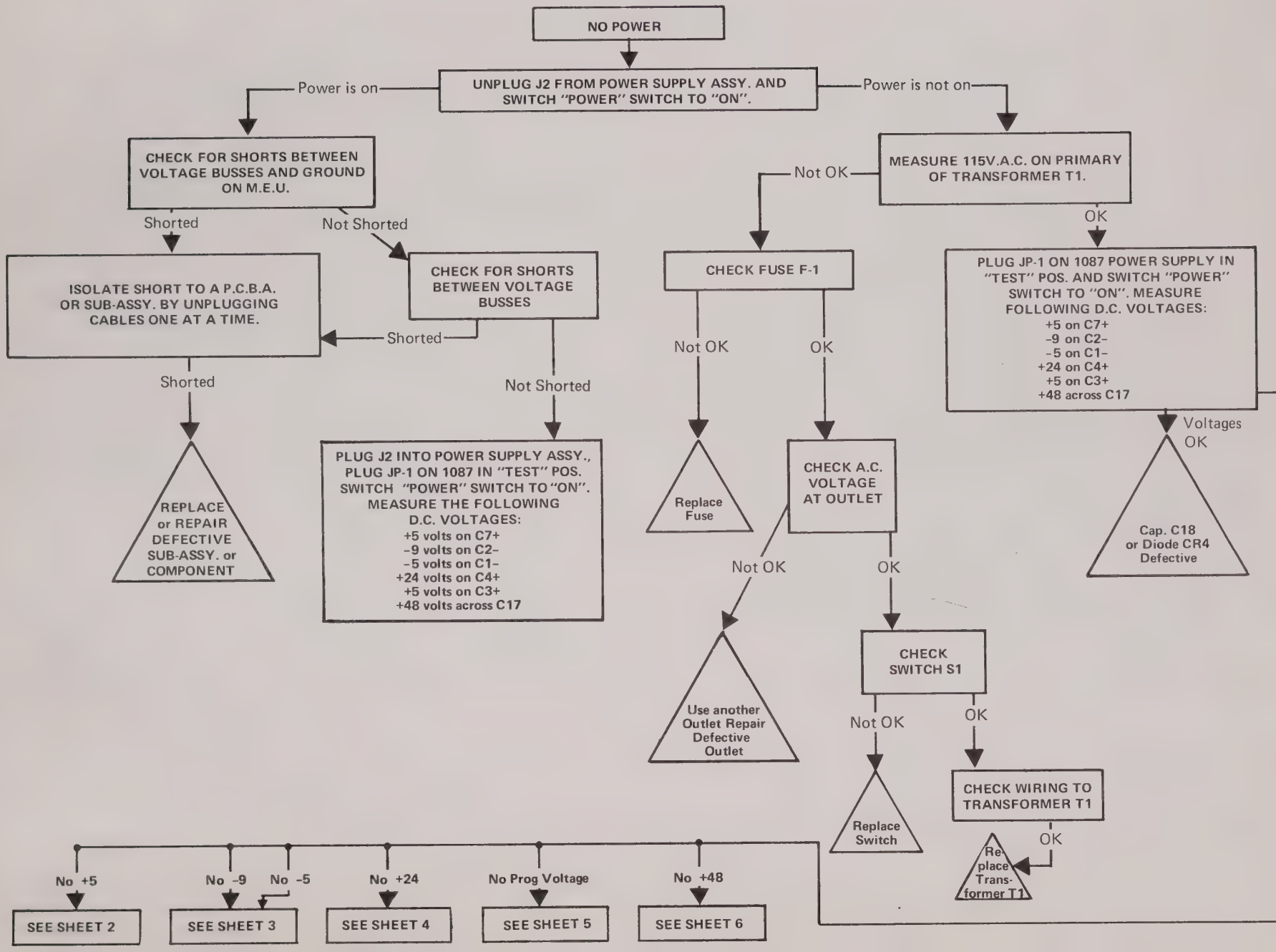
6.3.1 Regulated +5 Volts DC

Check the regulated +5 volt at Pads J or 8 of the MEU connectors (J3 through J9). If out of tolerance (+5 $\pm$0.1 volts), readjust the +5 reference volt adjustable potentiometer (R16) at the top center of the component side of the modular +5V Power Supply Circuit board.

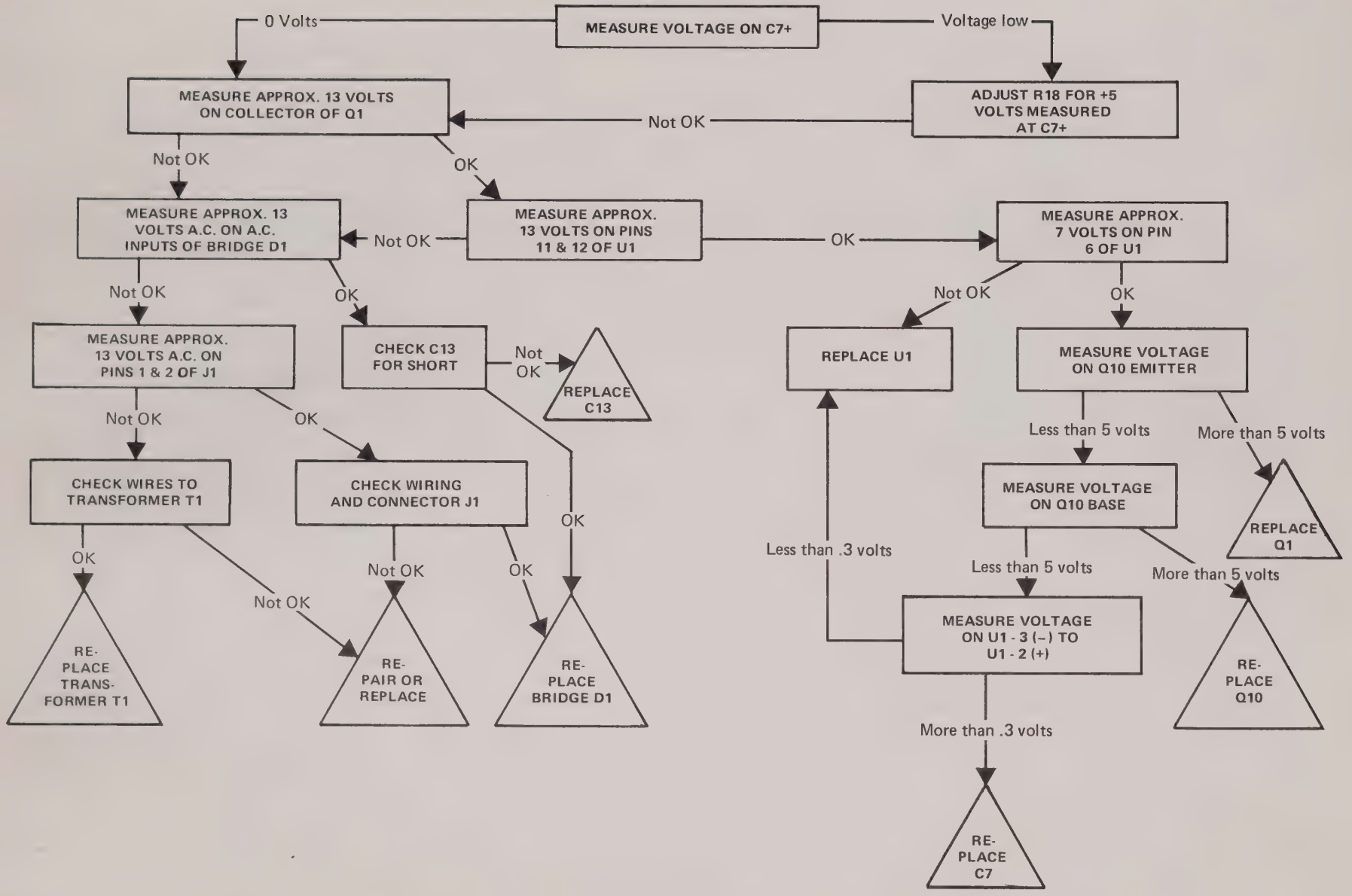
6.3.2 Regulated -9 Volts DC

Check the regulated -9 volts at Pads 7 or H of the MEU connectors (J3 through J8). If out of tolerance -9 +0.1 volts), readjust the -5 reference volt adjustable potentiometer (R15) at the top center of the component side of the modular +5V Power Supply Circuit board.

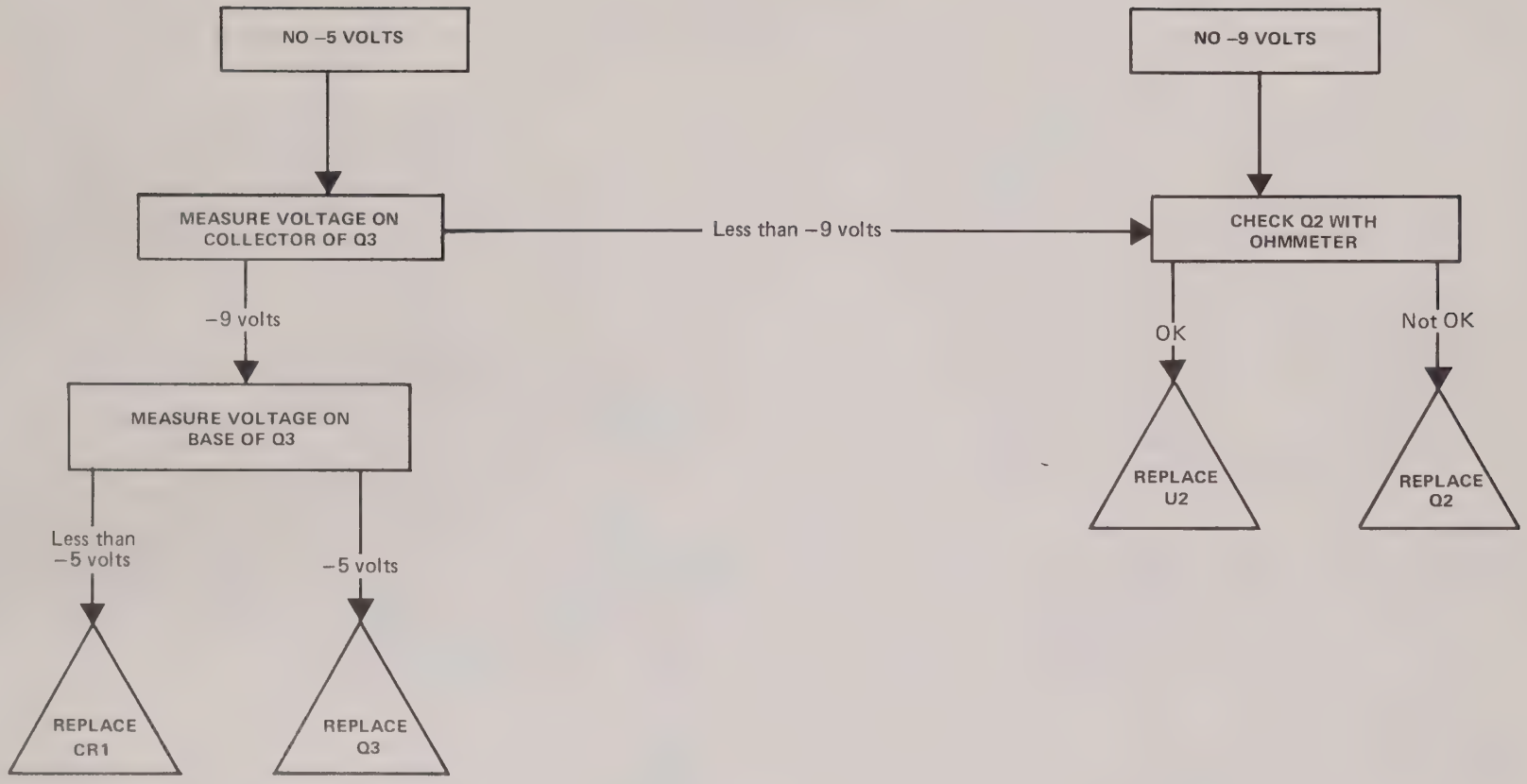
1087 POWER SUPPLY TROUBLESHOOTING DIAGRAMS


NO POWER
UNPLUG J2 FROM POWER SUPPLY ASSY. AND SWITCH "POWER" SWITCH TO "ON".
Power is on
Power is not on
CHECK FOR SHORTS BETWEEN VOLTAGE BUSSES AND GROUND ON M.E.U.
Shorted
Not Shorted
ISOLATE SHORT TO A P.C.B.A. OR SUB-ASSY. BY UNPLUGGING CABLES ONE AT A TIME.
Shorted
REPLACE or REPAIR DEFECTIVE SUB-ASSY. or COMPONENT
CHECK FOR SHORTS BETWEEN VOLTAGE BUSSES
Shorted
Not Shorted
PLUG J2 INTO POWER SUPPLY ASSY., PLUG JP-1 ON 1087 IN "TEST" POS. SWITCH "POWER" SWITCH TO "ON". MEASURE THE FOLLOWING D.C. VOLTAGES:
+5 volts on C7+
-9 volts on C2-
-5 volts on C1-
+24 volts on C4+
+5 volts on C3+
+48 volts across C17
MEASURE 115V.A.C. ON PRIMARY OF TRANSFORMER T1.
Not OK
OK
CHECK FUSE F-1
Not OK
OK
Replace Fuse
CHECK A.C. VOLTAGE AT OUTLET
Not OK
OK
Use another Outlet Repair Defective Outlet
CHECK SWITCH S1
Not OK
OK
Replace Switch
CHECK WIRING TO TRANSFORMER T1
OK
Re-place Trans-former T1
PLUG JP-1 ON 1087 POWER SUPPLY IN "TEST" POS. AND SWITCH "POWER" SWITCH TO "ON". MEASURE FOLLOWING D.C. VOLTAGES:
+5 on C7+
-9 on C2-
-5 on C1-
+24 on C4+
+5 on C3+
+48 across C17
Voltages OK
Cap. C18 or Diode CR4 Defective
Voltages Not OK
No +5
No -9
No -5
No +24
No Prog Voltage
No +48
SEE SHEET 2
SEE SHEET 3
SEE SHEET 4
SEE SHEET 5
SEE SHEET 6

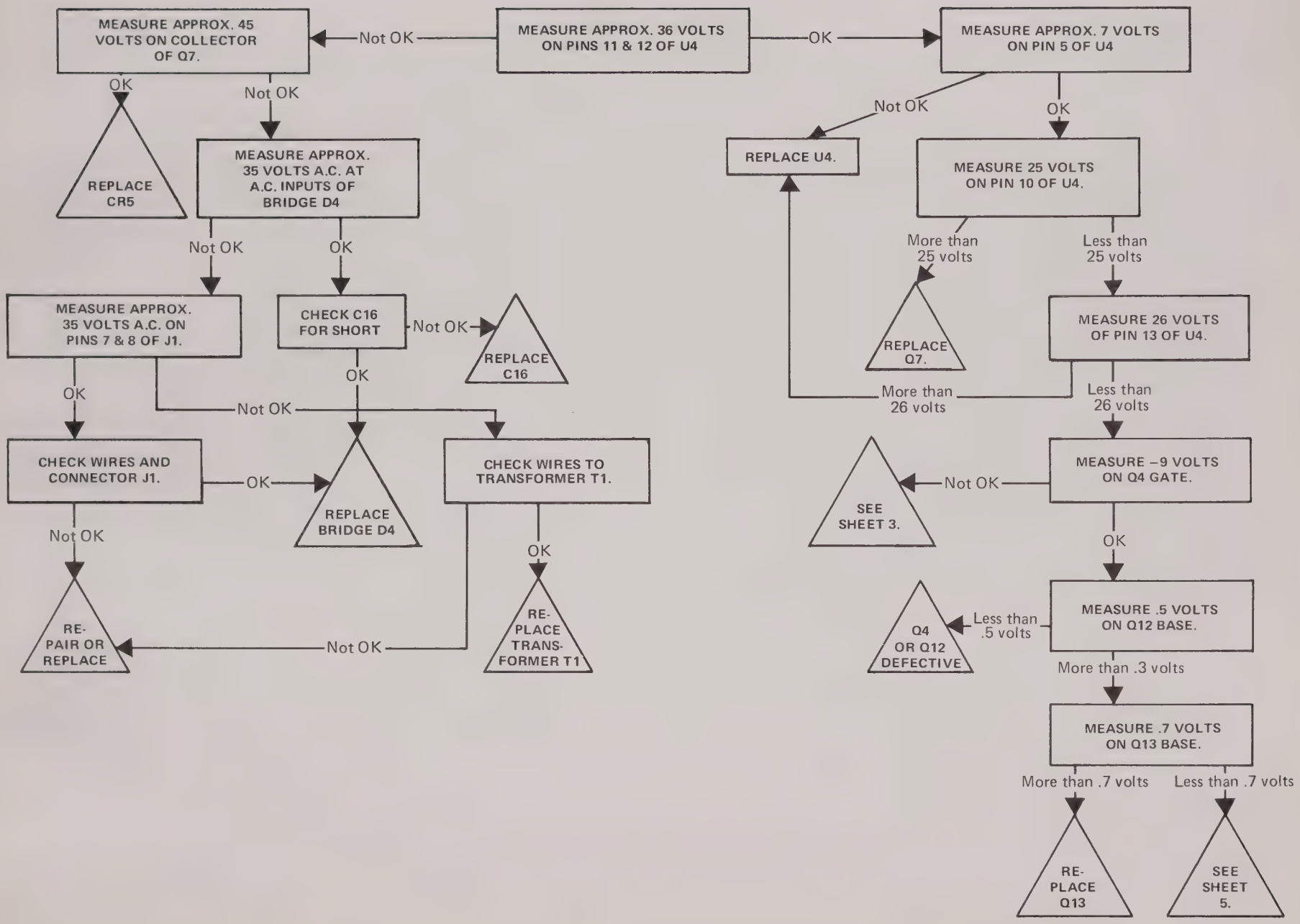
NO +5 VOLTS OR VOLTAGE TOO LOW



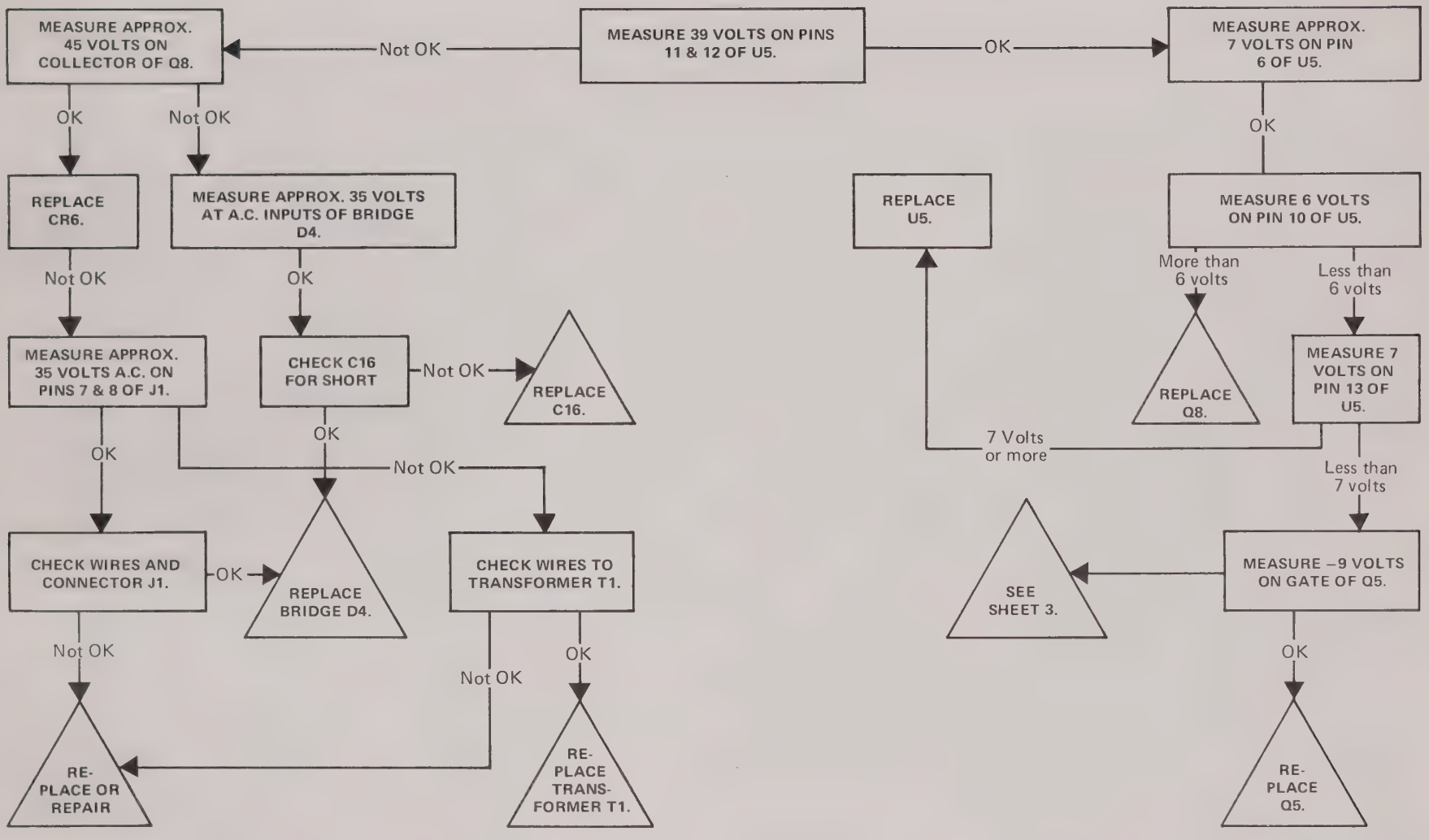
NO -9 VOLTS OR -5 VOLTS

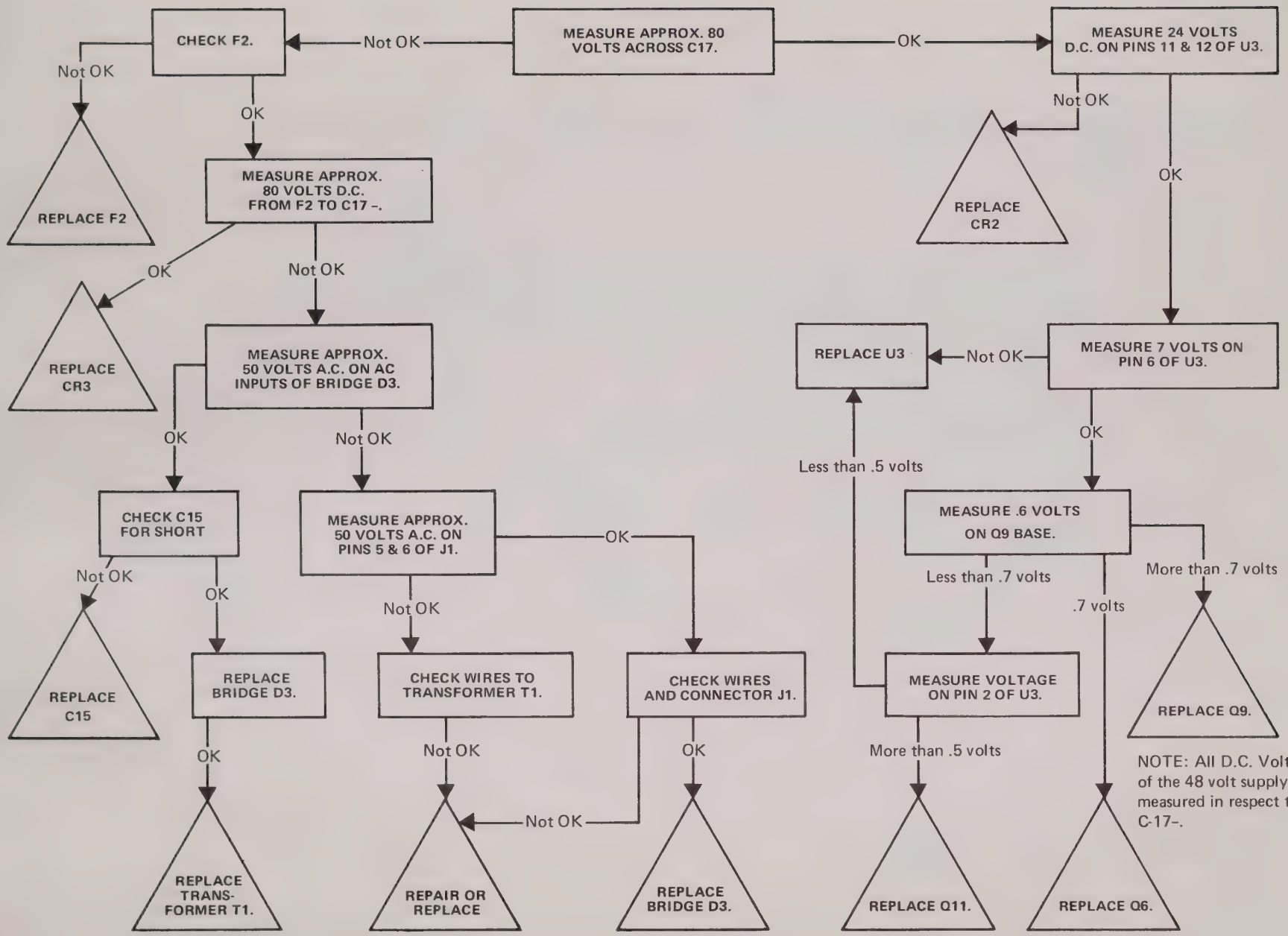


NO +24 VOLTS

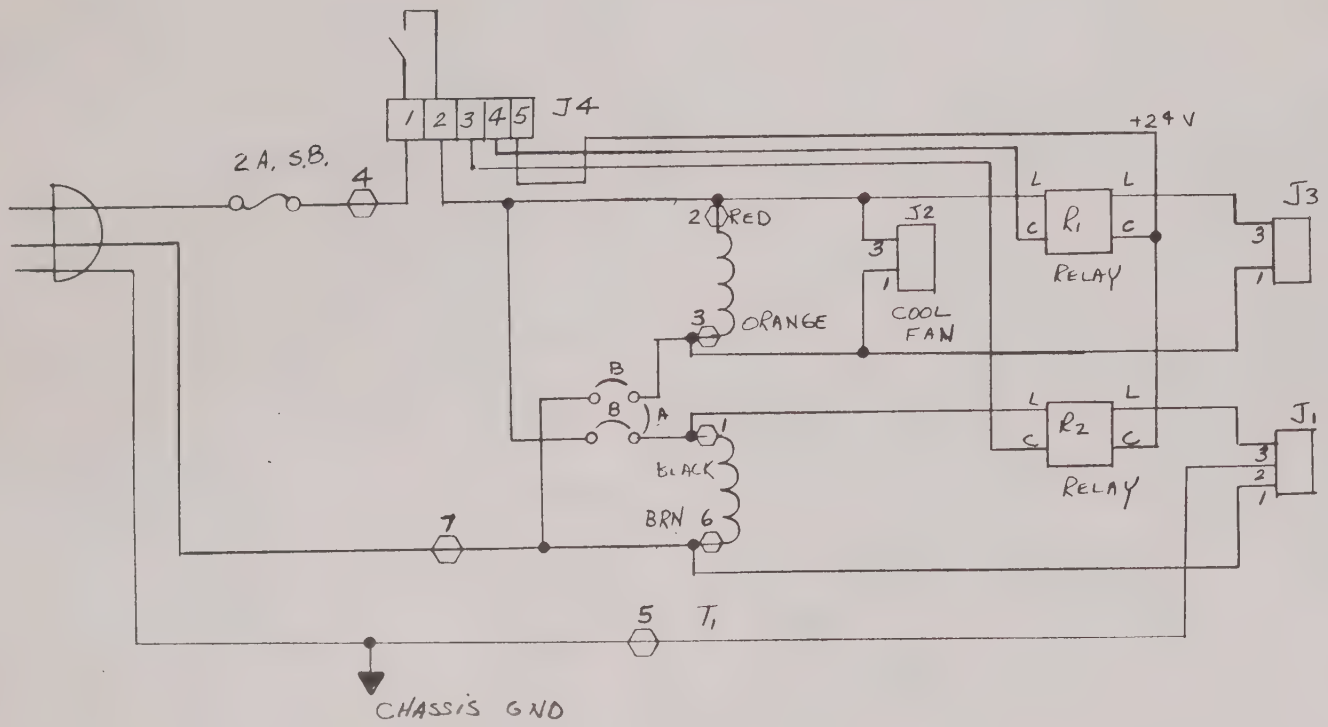

MEASURE APPROX. 45 VOLTS ON COLLECTOR OF Q7.
Not OK
MEASURE APPROX. 36 VOLTS ON PINS 11 & 12 OF U4
OK
MEASURE APPROX. 7 VOLTS ON PIN 5 OF U4
OK
REPLACE CR5
Not OK
MEASURE APPROX. 35 VOLTS A.C. AT A.C. INPUTS OF BRIDGE D4
Not OK
OK
MEASURE APPROX. 35 VOLTS A.C. ON PINS 7 & 8 OF J1.
CHECK C16 FOR SHORT
Not OK
REPLACE C16
OK
OK
Not OK
CHECK WIRES AND CONNECTOR J1.
OK
REPLACE BRIDGE D4
CHECK WIRES TO TRANSFORMER T1.
Not OK
OK
RE-PAIR OR REPLACE
Not OK
RE-PLACE TRANS-FORMER T1
Not OK
REPLACE U4.
OK
MEASURE 25 VOLTS ON PIN 10 OF U4.
More than 25 volts
Less than 25 volts
REPLACE Q7.
MEASURE 26 VOLTS OF PIN 13 OF U4.
More than 26 volts
Less than 26 volts
SEE SHEET 3.
Not OK
MEASURE –9 VOLTS ON Q4 GATE.
OK
Q4 OR Q12 DEFECTIVE
Less than .5 volts
MEASURE .5 VOLTS ON Q12 BASE.
More than .3 volts
MEASURE .7 VOLTS ON Q13 BASE.
More than .7 volts
Less than .7 volts
RE-PLACE Q13
SEE SHEET 5.

NO + PROGRAM VOLTAGE




MEASURE APPROX. 80 VOLTS ACROSS C17.
Not OK
CHECK F2.
Not OK
REPLACE F2
OK
MEASURE APPROX. 80 VOLTS D.C. FROM F2 TO C17 –.
OK
REPLACE CR3
Not OK
MEASURE APPROX. 50 VOLTS A.C. ON AC INPUTS OF BRIDGE D3.
OK
CHECK C15 FOR SHORT
Not OK
REPLACE C15
OK
REPLACE BRIDGE D3.
OK
REPLACE TRANS-FORMER T1.
Not OK
MEASURE APPROX. 50 VOLTS A.C. ON PINS 5 & 6 OF J1.
OK
CHECK WIRES AND CONNECTOR J1.
OK
REPLACE BRIDGE D3.
Not OK
CHECK WIRES TO TRANSFORMER T1.
Not OK
REPAIR OR REPLACE
OK
MEASURE 24 VOLTS D.C. ON PINS 11 & 12 OF U3.
Not OK
REPLACE CR2
OK
MEASURE 7 VOLTS ON PIN 6 OF U3.
Not OK
REPLACE U3
OK
MEASURE .6 VOLTS ON Q9 BASE.
Less than .5 volts
Less than .7 volts
MEASURE VOLTAGE ON PIN 2 OF U3.
More than .5 volts
REPLACE Q11.
.7 volts
More than .7 volts
REPLACE Q9.
REPLACE Q6.
NOTE: All D.C. Voltages of the 48 volt supply are measured in respect to C-17–.

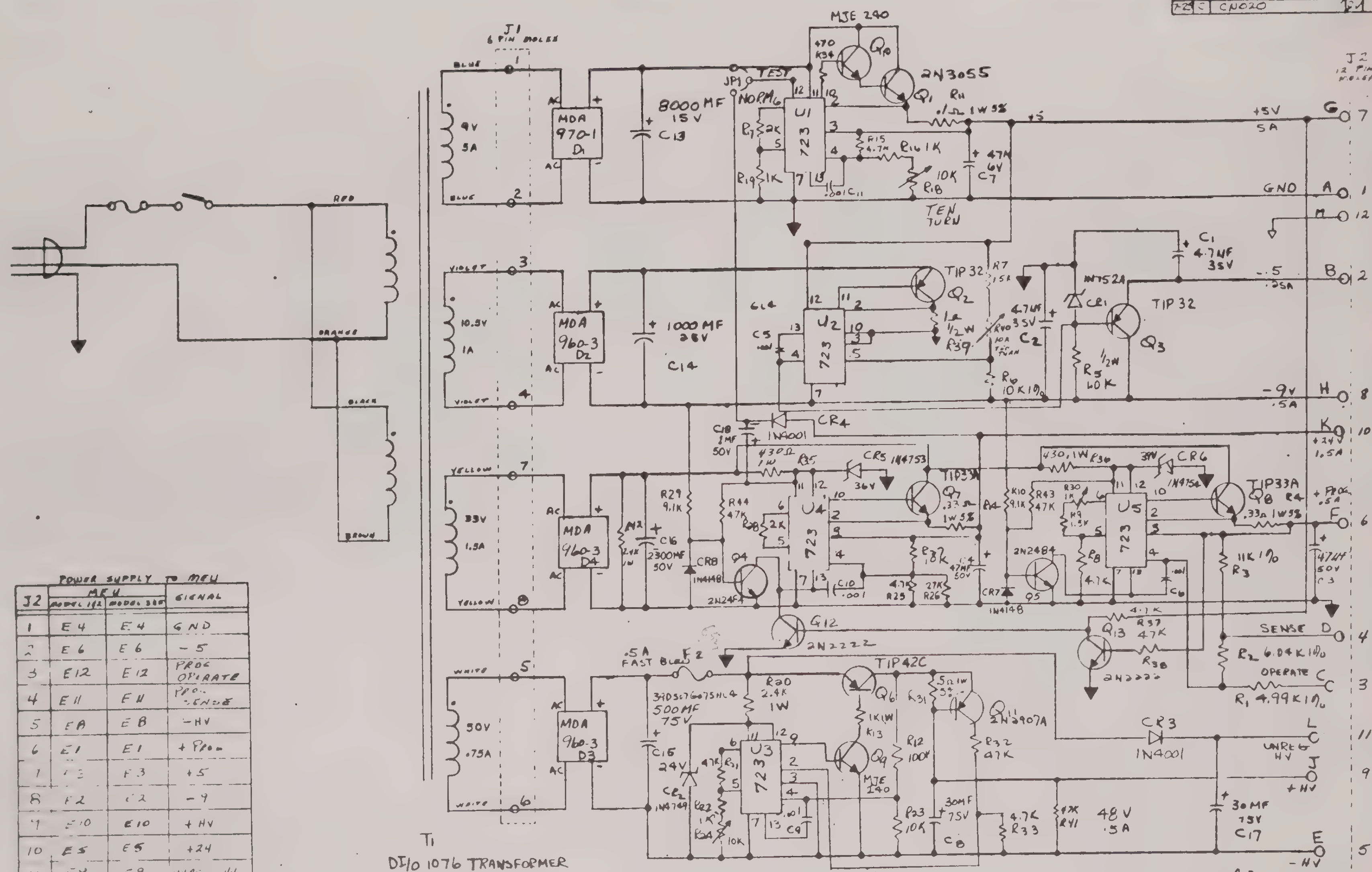
DATE	SYM	REVISION RECORD	DR	CK



TOLERANCES (EXCEPT AS NOTED)	DATA I/O BEL WN.		
DECIMAL ±		SCALE	DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE AC PWR DIST. - PROG1-2		
ANGULAR ±	DATE 3-25-74	DRAWING NUMBER 1109	

BRUNING 40-21

DATE	LTR	REVISION RECORD	DR	CK
7-8	H	CN006		
7-[illegible]	9	CN007		
7-2[illegible]	[illegible]	CN020		

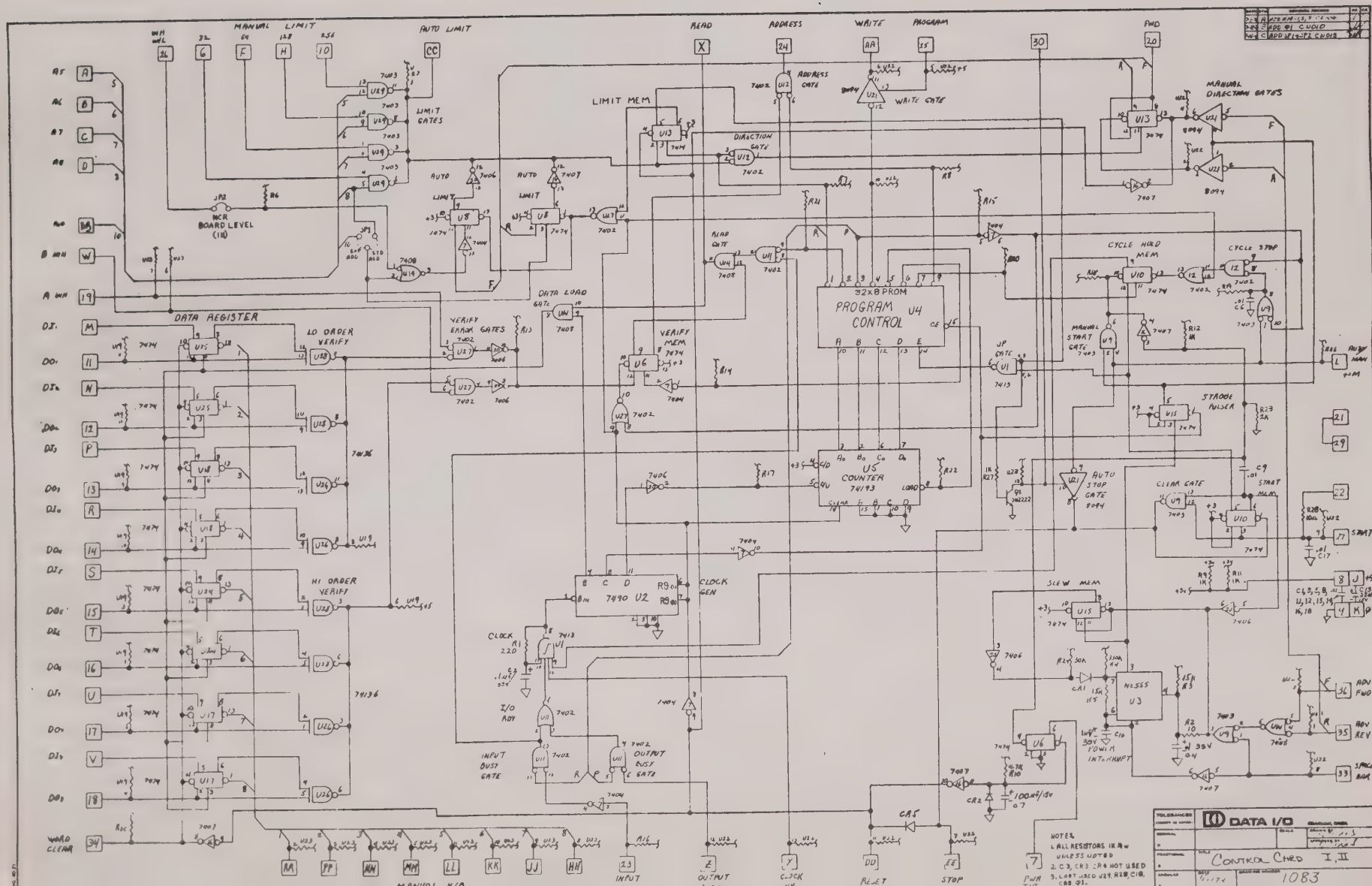


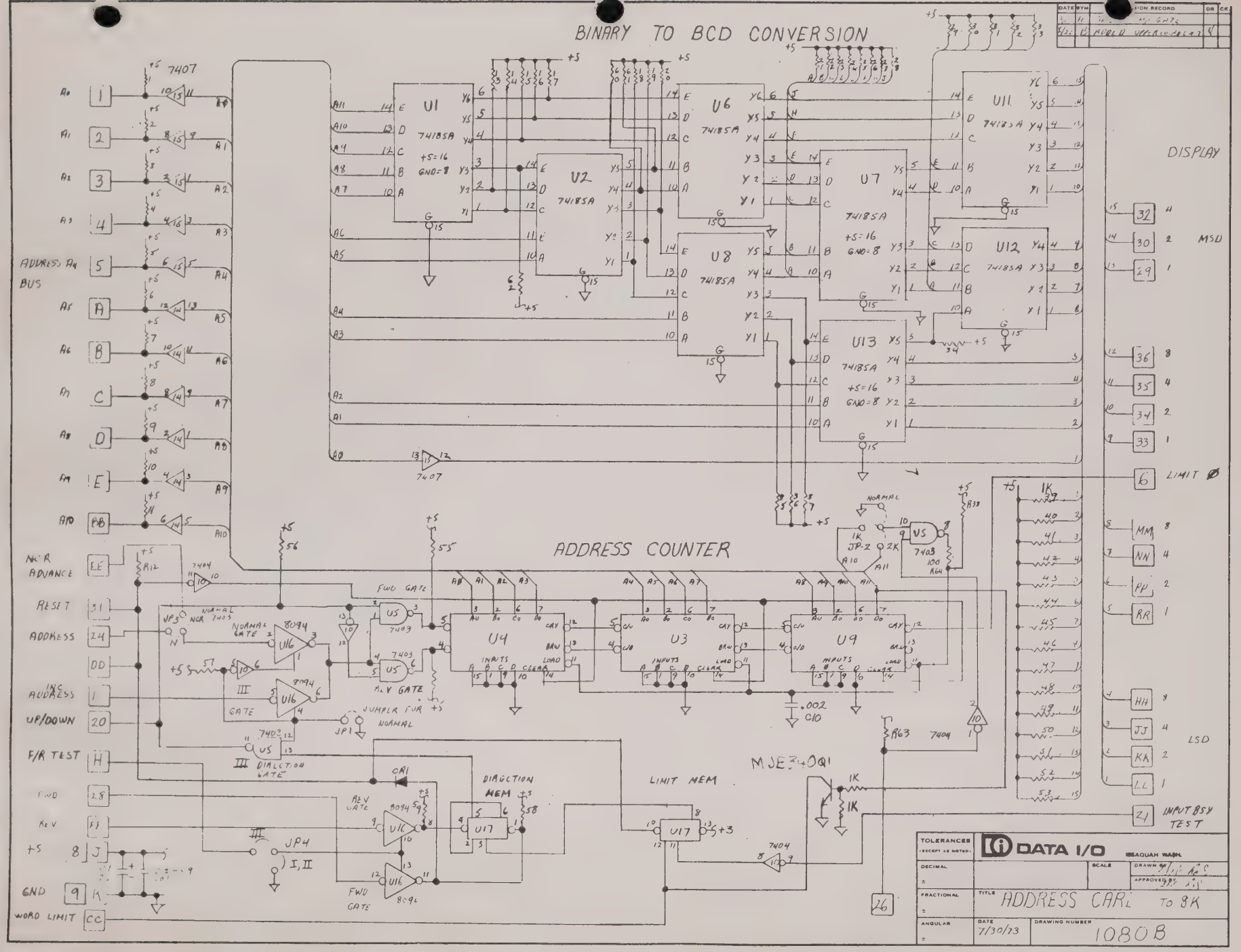
J2	MEH Model 1/2	MEH Model 300	SIGNAL
1	E4	E4	GND
2	E6	E6	-5
3	E12	E12	PROG OPERATE
4	E11	E11	PROG SENSE
5	E8	E8	-HV
6	E1	E1	+Prog
7	E3	E3	+5
8	E2	E2	-9
9	E10	E10	+HV
10	E5	E5	+24
11	E9	E9	UNREG. HV
12	E7	E7	GND

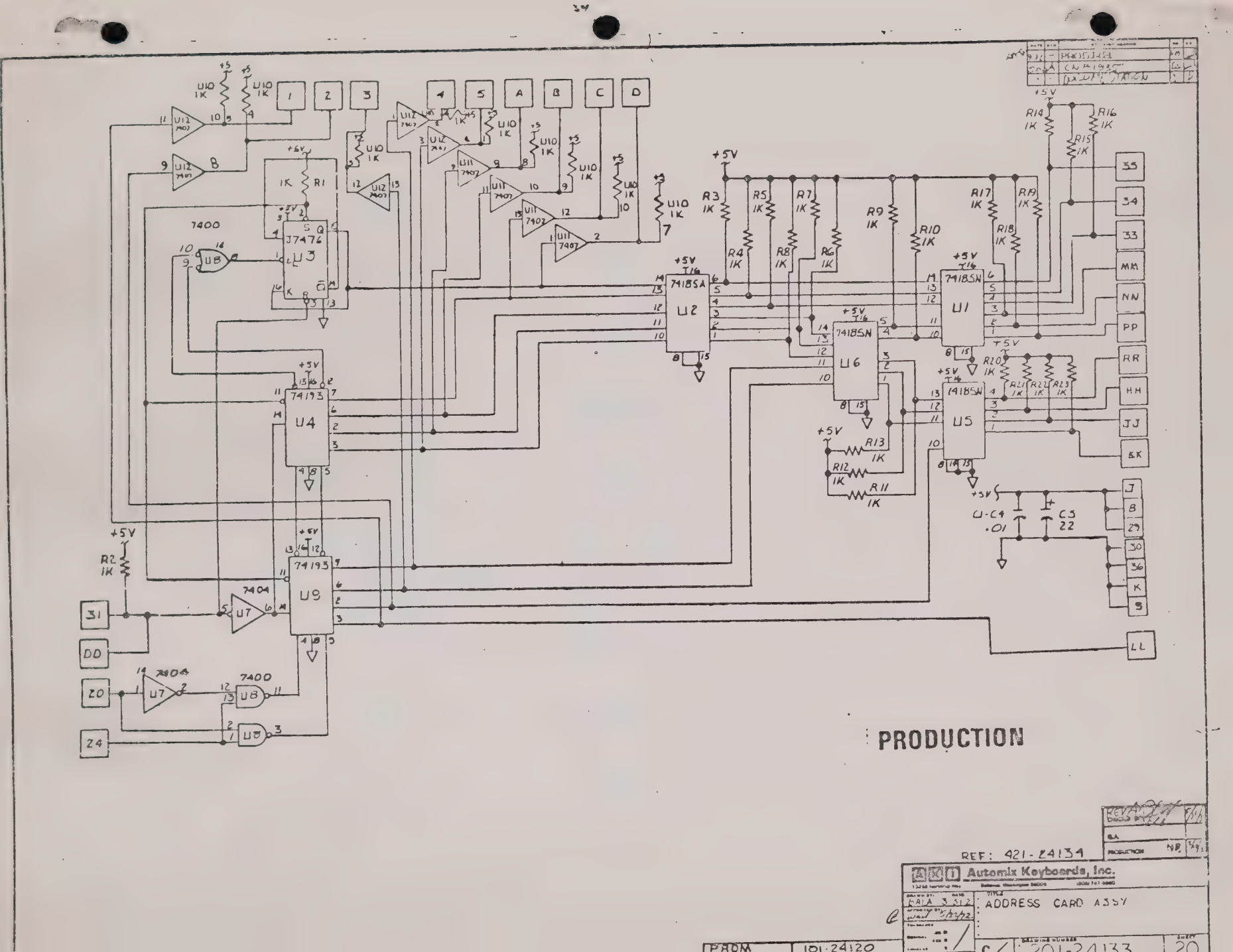
POWER SUPPLY TO MEH

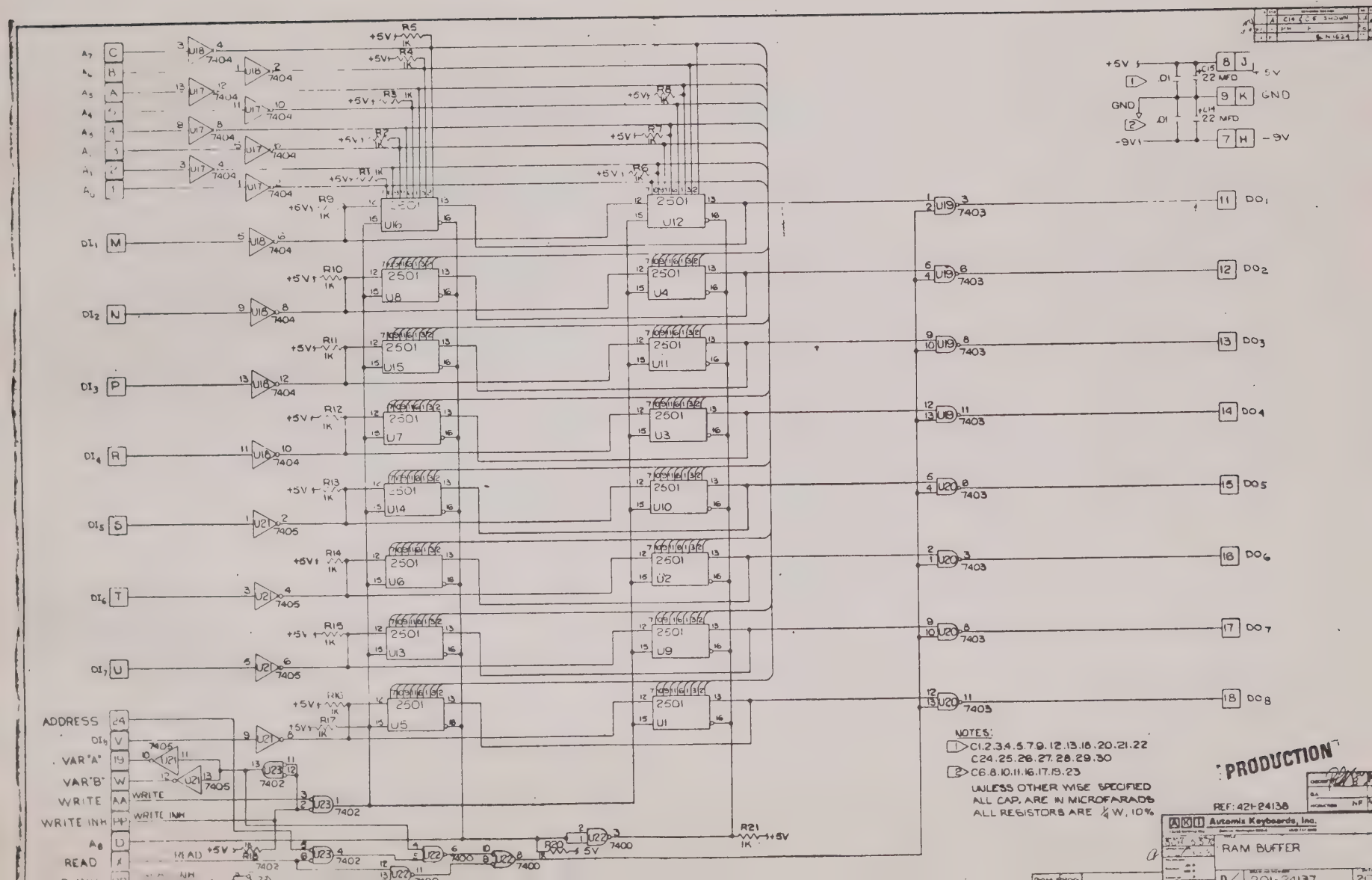
production Release MZ. 6-10-74

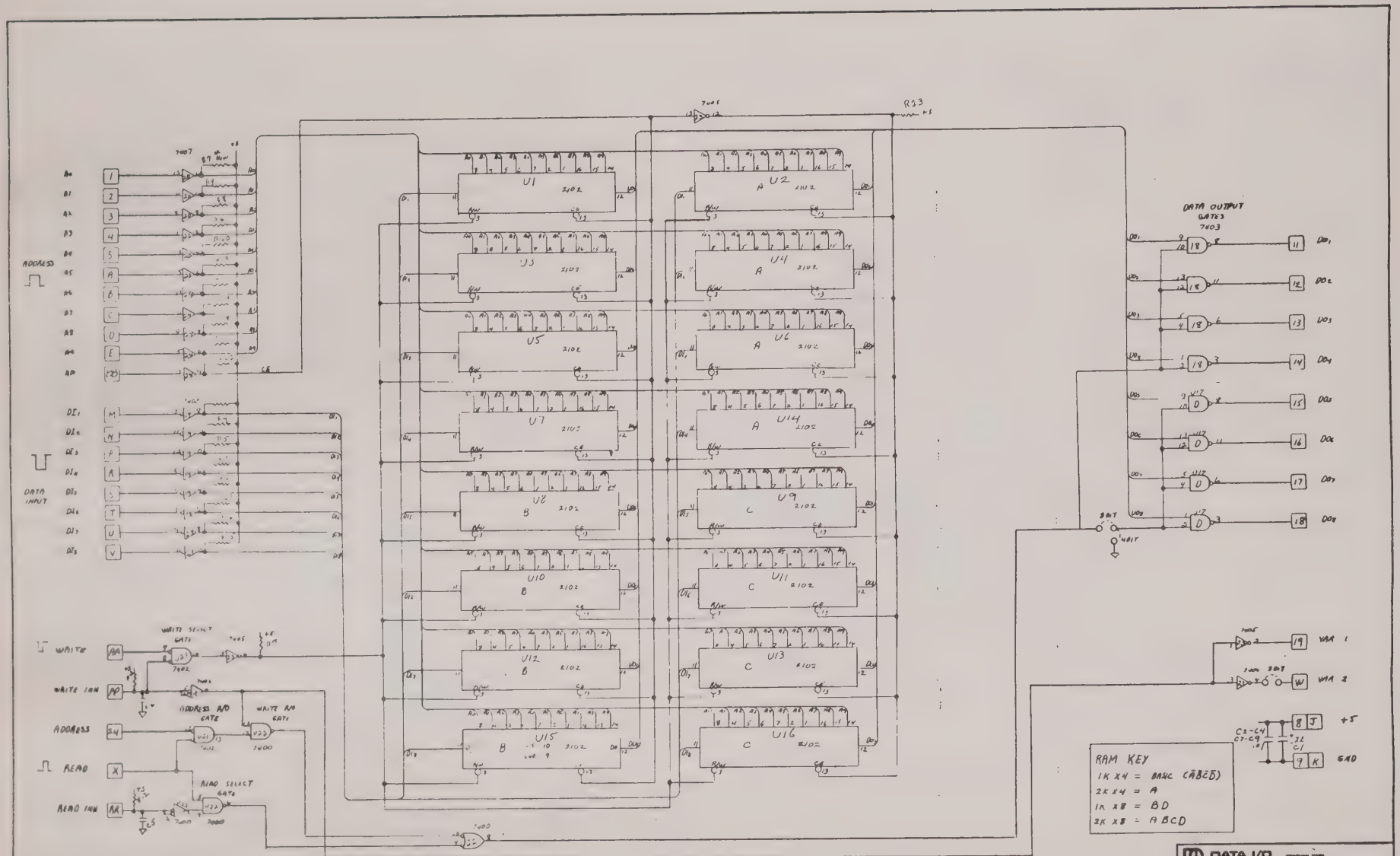
TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL		SCALE	DRAWN BY ME
			APPROVED BY
FRACTIONAL	TITLE PROG III PWR SUPPLY		
ANGULAR	DATE [illegible]-14	DRAWING NUMBER 1087	

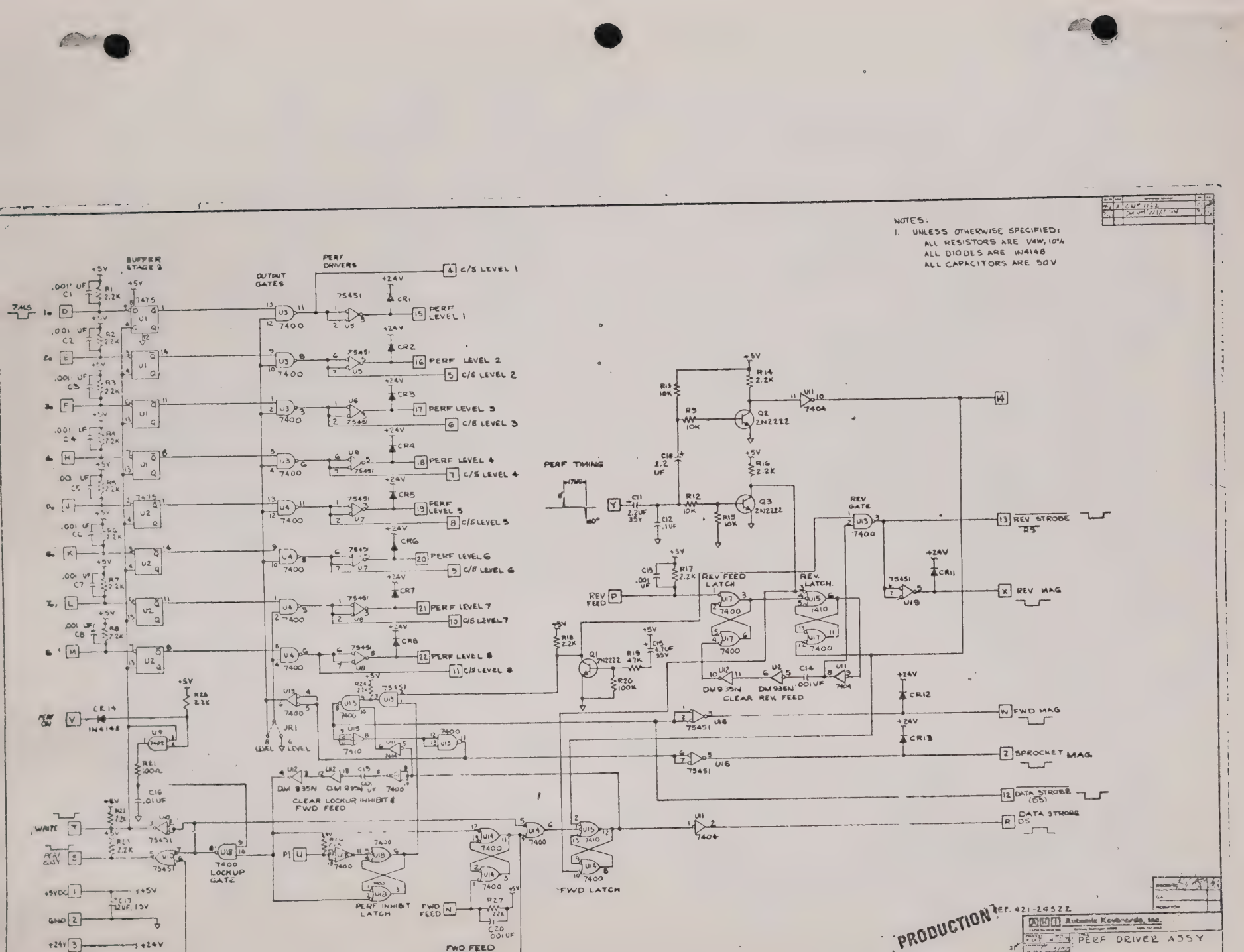

MANUAL LIMIT
AUTO LIMIT
LIMIT GATES
LIMIT MEM
READ
ADDRESS
WRITE
PROGRAM
FWD
ADDRESS GATE
WRITE GATE
DIRECTION GATE
MANUAL DIRECTION GATES
AUTO LIMIT
INCR BOARD LEVEL (11H)
DATA REGISTER
DATA LOAD GATE
VERIFY ERROR GATES
VERIFY MEM 7474
LO ORDER VERIFY
HI ORDER VERIFY
32X8 PROM
PROGRAM CONTROL U4
U5 COUNTER 74193
CYCLE HOLD MEM
CYCLE STOP
MANUAL START GATE 7403
JP GATE
STROBE PULSER
AUTO STOP GATE 8094
CLEAR GATE
SLEW MEM
CLOCK GEN
7490 U2
CLOCK
I/O ADV
INPUT BUSY GATE
OUTPUT BUSY GATE
NE555 U3
WORD CLEAR
INPUT
OUTPUT
CLOCK
RESET
STOP
DATA I/O
CONTROL CARD I, II
1083

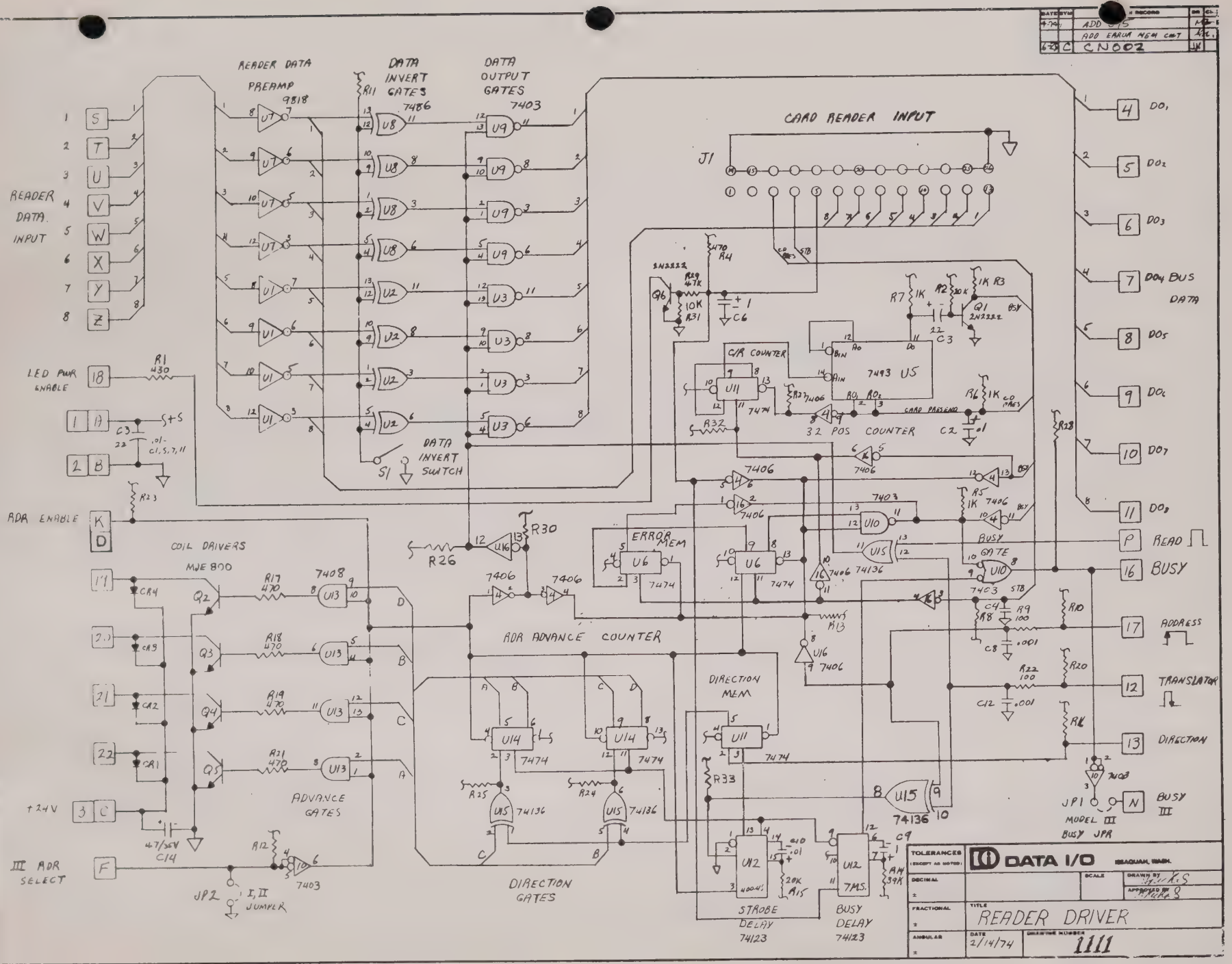

BINARY TO BCD CONVERSION
ADDRESS COUNTER
DISPLAY
ADDRESS BUS
7407
U1
U2
U6
U7
U8
U11
U12
U13
74185A
+5=16
GND=8
U4
U3
U9
INPUTS
CLEAR
LOAD
7403
7404
8094
MSD
LSD
LIMIT
INPUT BSY TEST
NORMAL ADVANCE
RESET
ADDRESS
INC ADDRESS
UP/DOWN
F/R TEST
FWD
REV
+5
GND
WORD LIMIT
FWD GATE
REV GATE
DIRECTION GATE
DIRECTION MEM
LIMIT MEM
JUMPER FOR NORMAL
MJE3904Q1
DATA I/O
REDMOND WASH.
ADDRESS CARL TO 8K
7/30/73
1080B


PRODUCTION
REF: 421-24134
Automix Keyboards, Inc.
ADDRESS CARD ASSY
421-24133
PROM 101-24120
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
74185A
74185N
74193
7400
7404
7407
J7476
+5V
1K
22
.01
I
2
3
4
5
A
B
C
D
7
31
DD
Z0
Z4
35
34
33
MM
NN
PP
RR
HH
JJ
KK
J
B
29
30
36
K
9
LL


+5V
GND
-9V
2501
7403
7404
7405
7402
7400
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
ADDRESS
VAR "A"
VAR "B"
WRITE
WRITE INH
READ
NOTES:
1 C1.2.3.4.5.7.9.12.13.18.20.21.22
C24.25.26.27.28.29.30
2 C6.8.10.11.16.17.23
UNLESS OTHER WISE SPECIFIED
ALL CAP. ARE IN MICROFARADS
ALL RESISTORS ARE ¼ W, 10%
PRODUCTION
REF: 421-24138
AKI Automix Keyboards, Inc.
RAM BUFFER

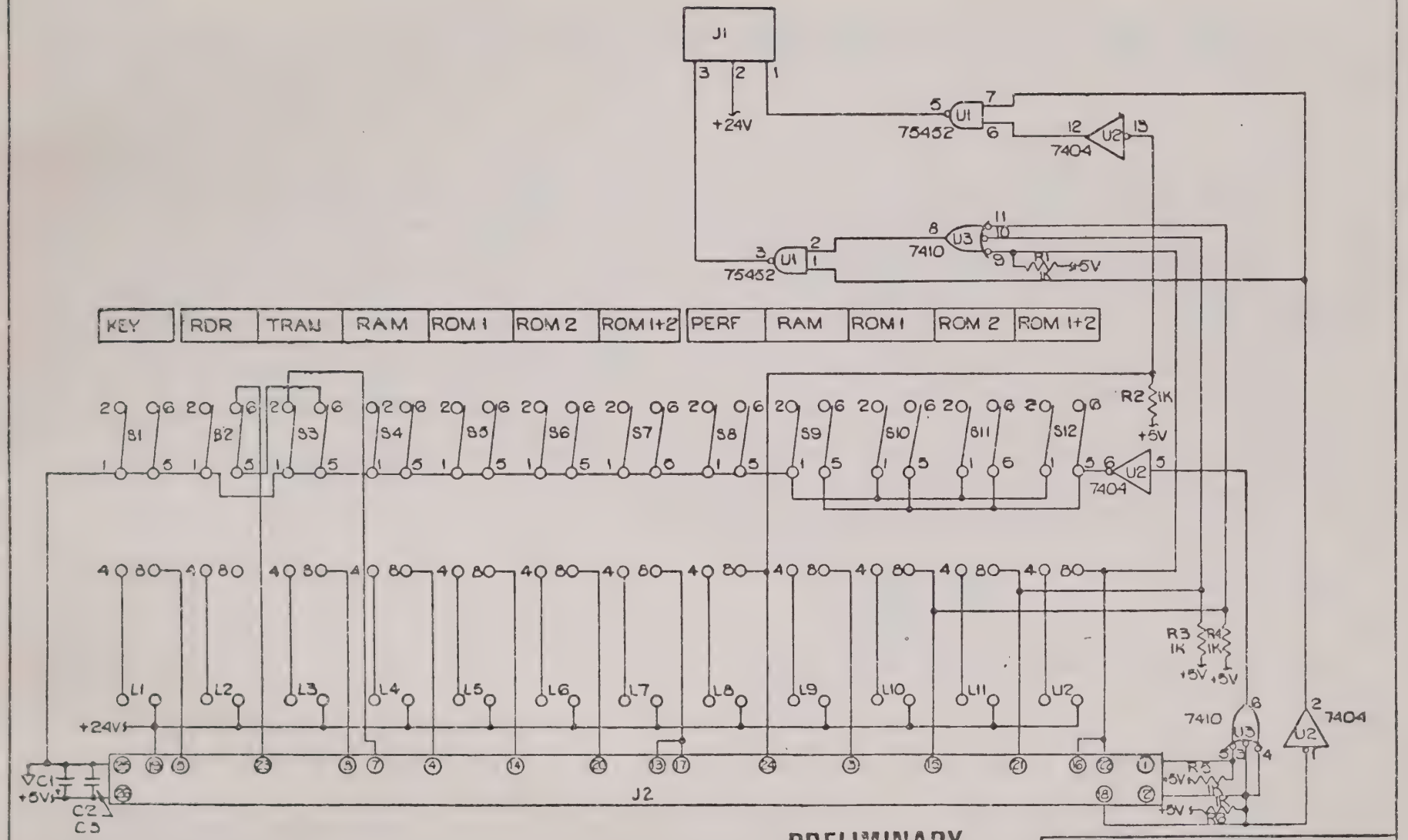

ADDRESS
DATA INPUT
WRITE
WRITE INH
ADDRESS
READ
READ INH
WRITE SELECT GATE
ADDRESS AND GATE
WRITE AND GATE
READ SELECT GATE
DATA OUTPUT GATES
7403
U1
U2
U3
U4
U5
U6
U7
U14
U8
U9
U10
U11
U12
U13
U15
U16
2102
A
B
C
RAM KEY
1K X4 = BASIC CABCD)
2K X4 = A
1K X8 = BD
2K X8 = ABCD
DATA I/O
RAM BUFFER
2K X8
1045


NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W, 10%
ALL DIODES ARE IN4148
ALL CAPACITORS ARE 50V
BUFFER STAGE 3
OUTPUT GATES
PERF DRIVERS
4 C/5 LEVEL 1
15 PERF LEVEL 1
16 PERF LEVEL 2
5 C/8 LEVEL 2
17 PERF LEVEL 3
6 C/8 LEVEL 3
18 PERF LEVEL 4
7 C/8 LEVEL 4
19 PERF LEVEL 5
8 C/8 LEVEL 5
20 PERF LEVEL 6
9 C/8 LEVEL 6
21 PERF LEVEL 7
10 C/8 LEVEL 7
22 PERF LEVEL 8
11 C/8 LEVEL 8
PERF TIMING
13 REV STROBE RS
X REV MAG
W FWD MAG
2 SPROCKET MAG
12 DATA STROBE (DS)
R DATA STROBE DS
REV FEED
REV LATCH
REV GATE
DM 835N
CLEAR REV FEED
CLEAR LOCKUP INHIBIT & FWD FEED
7400 LOCKUP GATE
PERF INHIBIT LATCH
FWD FEED
FWD LATCH
WRITE
+5VDC
GND
+24V
PRODUCTION
Ref. 421-24522
PERF DRIVER ASSY


READER DATA PREAMP 9818
DATA INVERT GATES 7486
DATA OUTPUT GATES 7403
CARD READER INPUT
READER DATA INPUT
LED PWR ENABLE
ADR ENABLE
COIL DRIVERS MJE 800
ADVANCE GATES
DIRECTION GATES
ADR ADVANCE COUNTER
ERROR MEM
DIRECTION MEM
C/R COUNTER
7493 U5
32 POS COUNTER
CARD PASSING
DATA INVERT SWITCH
S1
JP2 I, II JUMPER
III ADR SELECT
JP1 MODEL III BUSY JPR
STROBE DELAY 74123
BUSY DELAY 74123
DO1
DO2
DO3
DO4 BUS DATA
DO5
DO6
DO7
DO8
READ
BUSY
ADDRESS
TRANSLATOR
DIRECTION
BUSY III
DATA I/O
READER DRIVER
2/14/74
1111

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE 1/4W, 10%.
   ALL CAPACITORS ARE .01MFD, 50V, 10%

REV		
A		UPDATE DWG
B		UPDATE DWG



PRELIMINARY PRODUCTION

REF: 421-24130

ROM PROG	101-24120

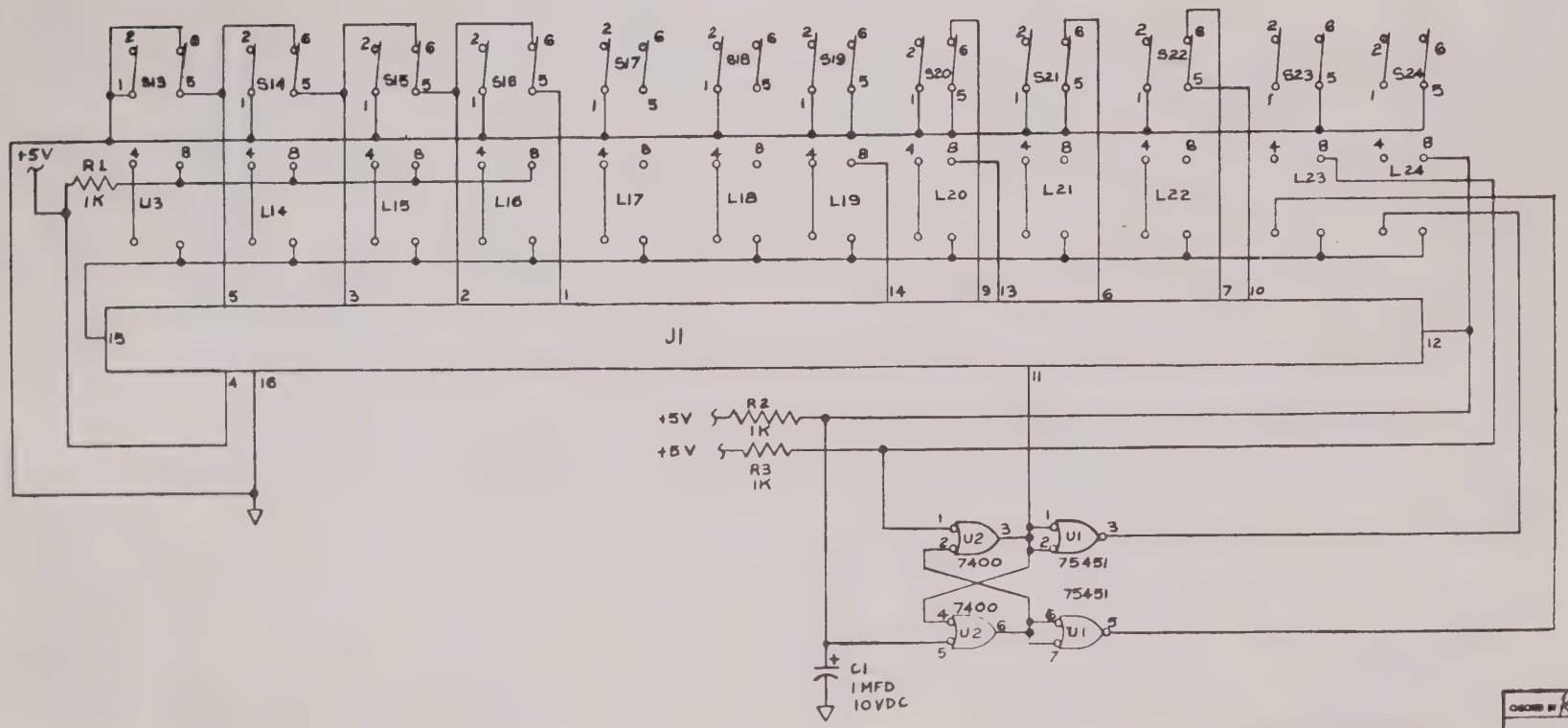
Automix Keyboards, Inc.

CONTROL SWITCH ASSY

201-24129

B	ADDED C1	
A	PROD. REL	

32	64	128	256	512	INSERT	VERIFY	PROGRAM	MANUAL	AUTO	START	STOP



PRODUCTION

CHECKED BY		
Q.A.		
PRODUCTION		

NOTE:
UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE ¼W ± 10%.

REF: 421-24546

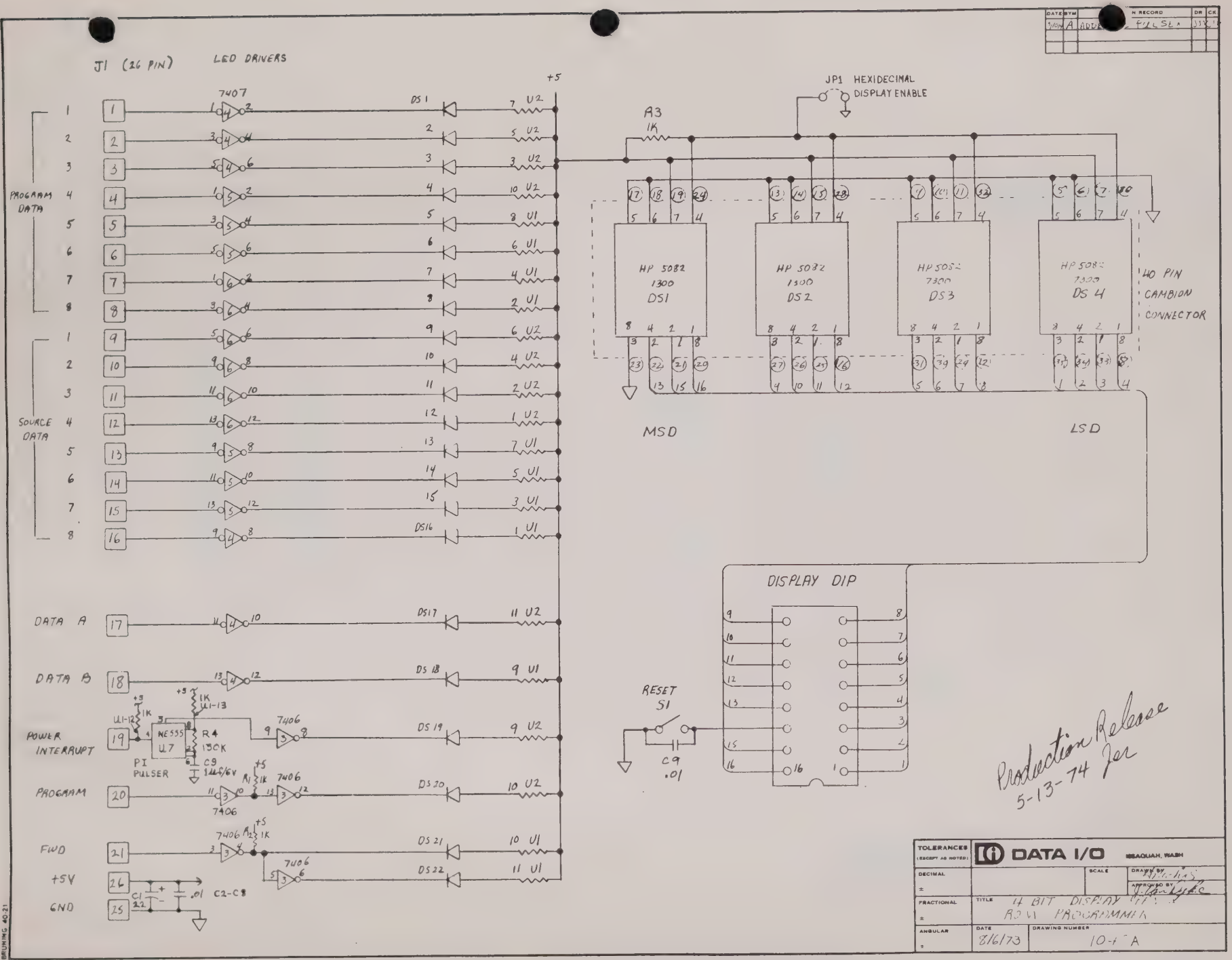
Automix Keyboards, Inc.

DRAWN BY	DATE
GFC	5-92
APPROVED BY	DATE
	2/22/78

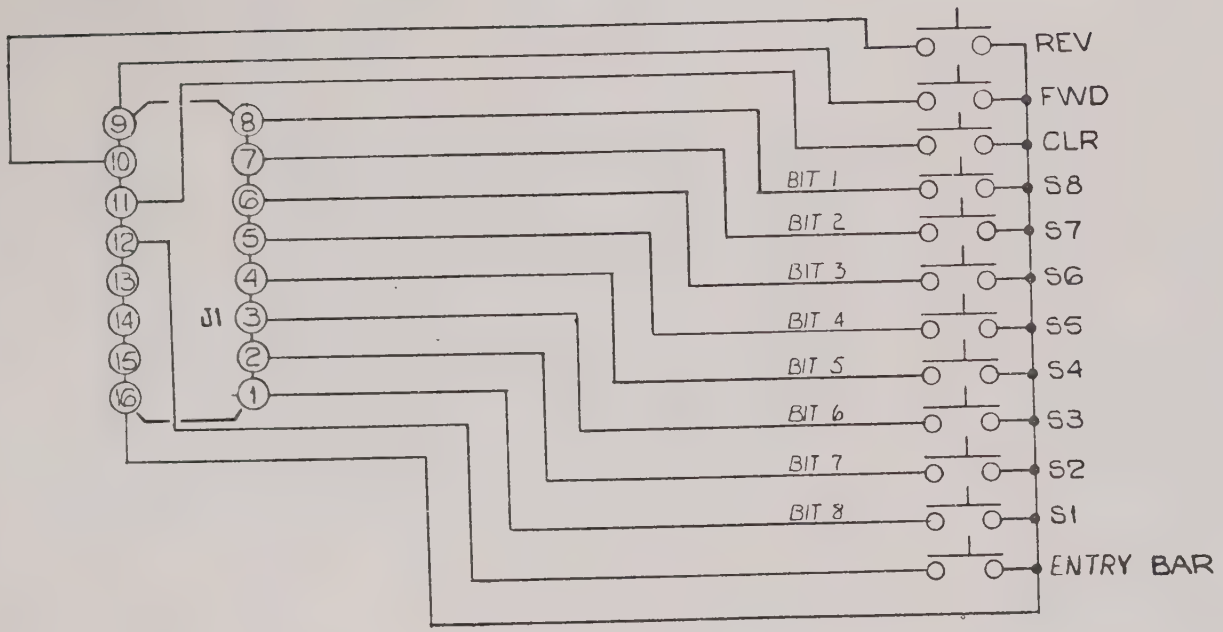
TITLE: MODE SWITCH ASSY. ROM PROGRAMMER

ROM PROG	101-24120
SYSTEM	
	NONE

C | DRAWING NUMBER 201-24545 | SHEET 20


J1 (26 PIN)
LED DRIVERS
7407
+5
PROGRAM DATA
SOURCE DATA
DS1
DS16
DS17
DS18
DS19
DS20
DS21
DS22
DATA A
DATA B
POWER INTERRUPT
PROGRAM
FWD
+5V
GND
NE555
U7
R4
130K
C9
PI PULSER
7406
C1
22
.01
C2-C8
A3
1K
JP1 HEXIDECIMAL DISPLAY ENABLE
HP 5082 1300 DS1
HP 5082 1300 DS2
HP 5082 7300 DS3
HP 5082 7300 DS 4
40 PIN CAMBION CONNECTOR
MSD
LSD
DISPLAY DIP
RESET S1
C9 .01
Production Release 5-13-74 JCR
DATA I/O
REDMOND, WASH
TITLE 4 BIT DISPLAY W/ R.A.M. PROGRAMMER
DATE 8/6/73
DRAWING NUMBER 10-1 A
BRUNING 40-21

DATE	SYM	REVISION RECORD	DR	CK
9/9/82	-	PROD. REL.	EA	
11/	-	DOCUMENTATION		JVC

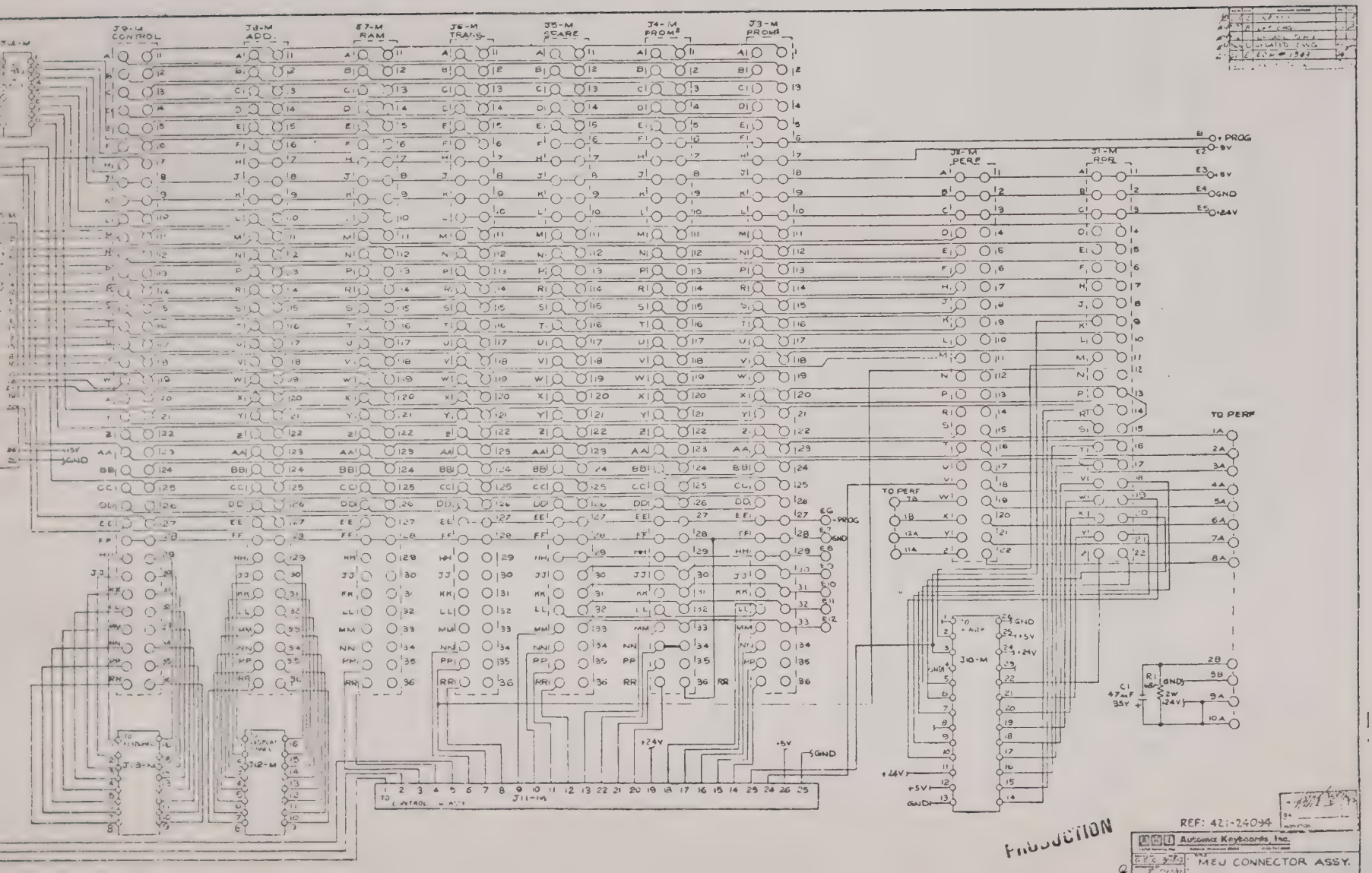


CHECKED BY	RDW	9/9/82
Q.A.		
PRODUCTION	JVC	9/1/82

Automix Keyboards, Inc.
13256 Northrup Way Bellevue, Washington 98005 (206) 747-6980

DRAWN BY: G.E.C. DATE	TITLE: KEYBOARD SWITCH ASSY.
APPROVED BY: DR. F 7/21/82	
TOLERANCES: DECIMAL .XX ±, .XXX ±, ANGULAR ±	DRAWING NUMBER: B / 212-23799
	SHEET 20

ROM PROG	101-24124&24930



PRODUCTION

Automax Keyboards, Inc.

MEU CONNECTOR ASSY.

DATA I/O

SERVICE POLICY

A. SERVICE DURING THE FIRST 90 DAYS

1. Data I/O shall repair or replace, at Data I/O's discretion, any new system for a period of 90 days and any used system for a period of 30 days from the date of installation found to be defective.

   This service will be provided at no extra charge and within a reasonable amount of time after notification by the purchaser to Data I/O of a malfunction. This service shall not apply to equipment that has been subject to abuse, misuse, negligence or accident or to which any modification, alterations or attachments have been made without the written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in a location not free from excessive dirt, dust, moisture, fumes, or extremes in temperature.

2. The warranty period is effective as of the date 10 days following actual shipping.

3. This warranty policy is in lieu of all other warranties, expressed or implied, unless warranty extensions are granted by Data I/O in writing.

B. SERVICE AFTER 90 DAY WARRANTY PERIOD EXPIRES

1. **Service Calls:**

   Service calls will be billed at the rates of $ 20 per hour for labor and $20 per hour for travel, portal-to-portal. It will be at Data I/O's discretion whether to attempt to correct a problem by telephone or send a Service Engineer for in-plant repair.

2. **Service Calls After Hours And On Saturdays, Sundays, And National Holidays**

   Time and one-half rate shall apply. Normal hours are Monday through Friday, 8:30 A.M. to 5:00 P.M.

   The customer will not be charged time and one-half for service calls that start during normal work hours and continue into the overtime period if access to the equipment is granted by 3:00 P.M. on the day service is scheduled.

3. **Installation Of Modification Kits Or Customer Requested Changes**

   Cost of any engineering charges, cost of parts, plus cost of time spent installing the item, is billed at standard rates.

C. WARRANTY ON PARTS

1. Data I/O warrants electronic components of programmer systems to be free from defects in material and workmanship under normal use. Data I/O's obligation under this warranty shall extend for a period of one (1) year on new systems and for a period of ninety (90) days on used systems and shall be limited to replacing or repairing, at Data I/O's discretion and at no charge to the purchaser, any parts which on examination by Data I/O shall be found defective.

2. Data I/O warrants mechanical components to be free from defects in material and workmanship under normal use.

Data I/O's obligation under this warranty shall extend for a period of ninety (90) days on new systems and thirty (30) days on used systems and shall be limited to replacing or repairing at Data I/O's discretion and at no charge to the purchaser any part which on examination by Data I/O shall be found defective.

3. Lamps, fuses, and other limited life components shall be considered expendable components to which the warranty period shall be limited to thirty (30) days, except where evidence of damage caused by the customer by misuse, negligence, or other reason (listed in paragraph A.1) is present.

4. For any equipment modified or rebuilt under the direction of Data I/O, the warranty period extends ninety (90) days for both service and parts excluding used systems which are covered under sections A.1 and C.1, C.2.

D. PARTS RETURNED TO DATA I/O BY THE CUSTOMER FOR REPAIR OR REPLACEMENT

1. **During The Warranty Period:**

No charge for replacement or repair of parts under warranty, except that the defective parts must be shipped to Data I/O prepaid.

2. **After The Warranty Period Expires:**

Time, material, and cost of shipping. Time is charged at $ 10 per hour.

3. **Ordering Instructions:**

The order should contain the following information:

Description of part(s) and Data I/O part number(s).

Quantity of each item to be ordered.
Serial number of programmer and the model number.
Corporate name of firm.
Shipping address of firm, including zip code.
Full name of person ordering the part(s).
To whose attention the part(s) are to be shipped.
Any special billing information.
Purchase order number where applicable.

4. **Shipping Instructions:**

When returning a part(s), please follow these instructions:

Parts are to be send prepaid in all instances.
Item being returned should have a cover letter or enclosure explaining the reason why they are being returned and the action that Data I/O is requested to take, including:

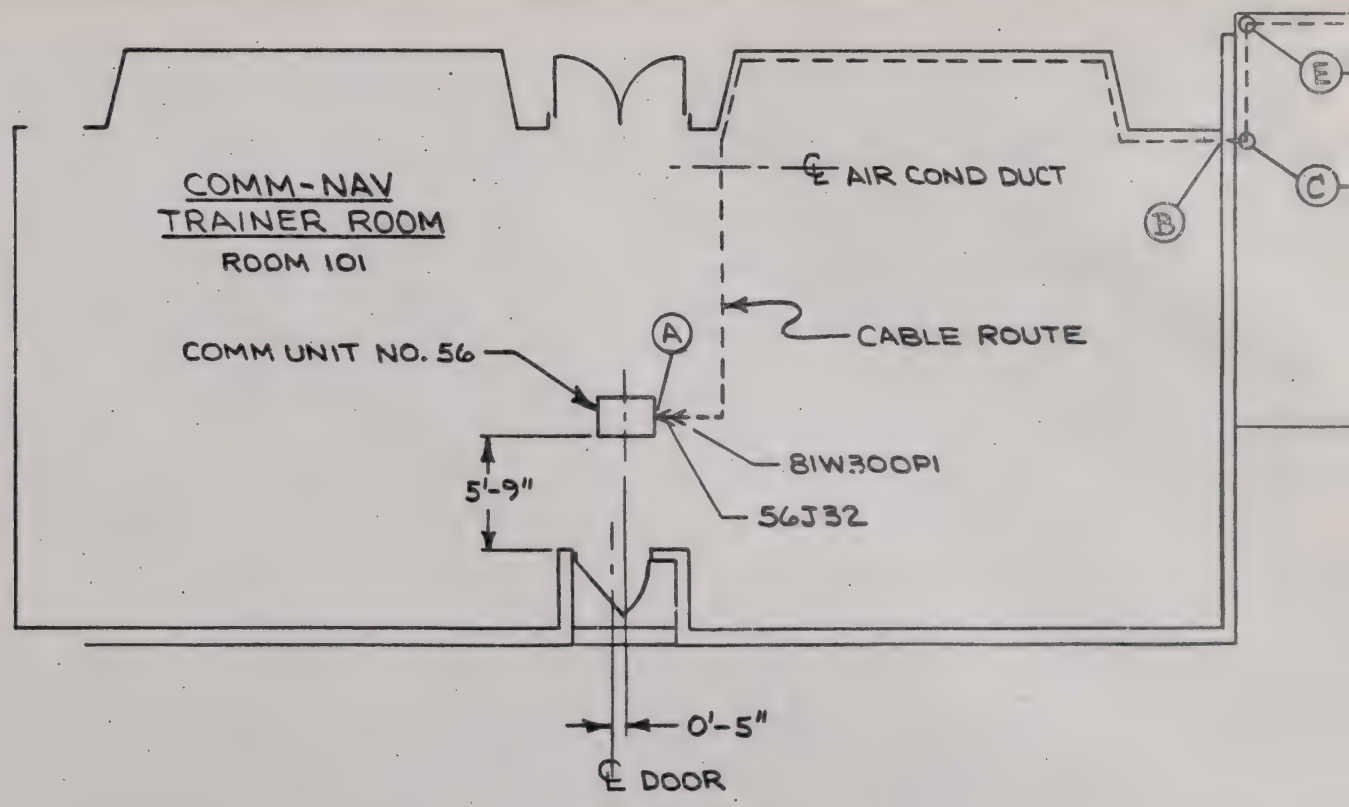
The corporate name of firm.
Shipping address of firm returning the part(s).
To whose attention a replacement part must be sent.

Send all part(s) to DATA I/O
12841 N. E. 14th PLACE
BELLEVUE, WASHINGTON 98005
ATTENTION: SERVICE DEPARTMENT

RTG SYM	CABLE ROUTING, CABLE NO. 81W300
(A)	CABLE CONNECTOR 56J32 ON LEFT FACE OF UNIT 56 CABLE BUCKET BELOW ELEV FLR LEVEL
(A) TO (B)	ROUTE BELOW ELEV FLR & OVER TOP OF A/C DUCT AT DUCT - CABLE INTERSECTION INDICATED
(B) TO (C)	PENETRATE 8" CONCRETE BLOCK WALL BELOW ELEVATED FLOOR LEVEL
(C) TO (D)	CABLE RISES VERTICALLY UP RM 102 WALL APPROX 6 FT TO UNDERSIDE OF OUTSIDE AIR INTAKE DUCT
(D) TO (E)	ROUTE CABLE HORIZONTALLY ON WALL BELOW DUCT TO CORNER OF ROOM
(E) TO (F)	CABLE RISES VERTICALLY UP WALL TO NEAR CEILING LEVEL (9'-10" HIGH CEILING)
(F) TO (G)	ROUTE CABLE HORIZONTALLY ON WALL ACROSS ROOM
(G) TO (H)	PENETRATE 8" CONCRETE BLOCK WALL BELOW 9'-4" GYPSUM PLASTER CEILING IN RM 104
(H) TO (I)	ROUTE CABLE HORIZONTALLY ON RM 104 WALL NEAR AND BELOW 9'-4" CEILING

RTG SYM	CABLE RO
(I) TO (J)	DROP CAB ACROSS THRU GR PANEL, INTERNA & TERM

FOLD



FOLD

4 | 3 | 2

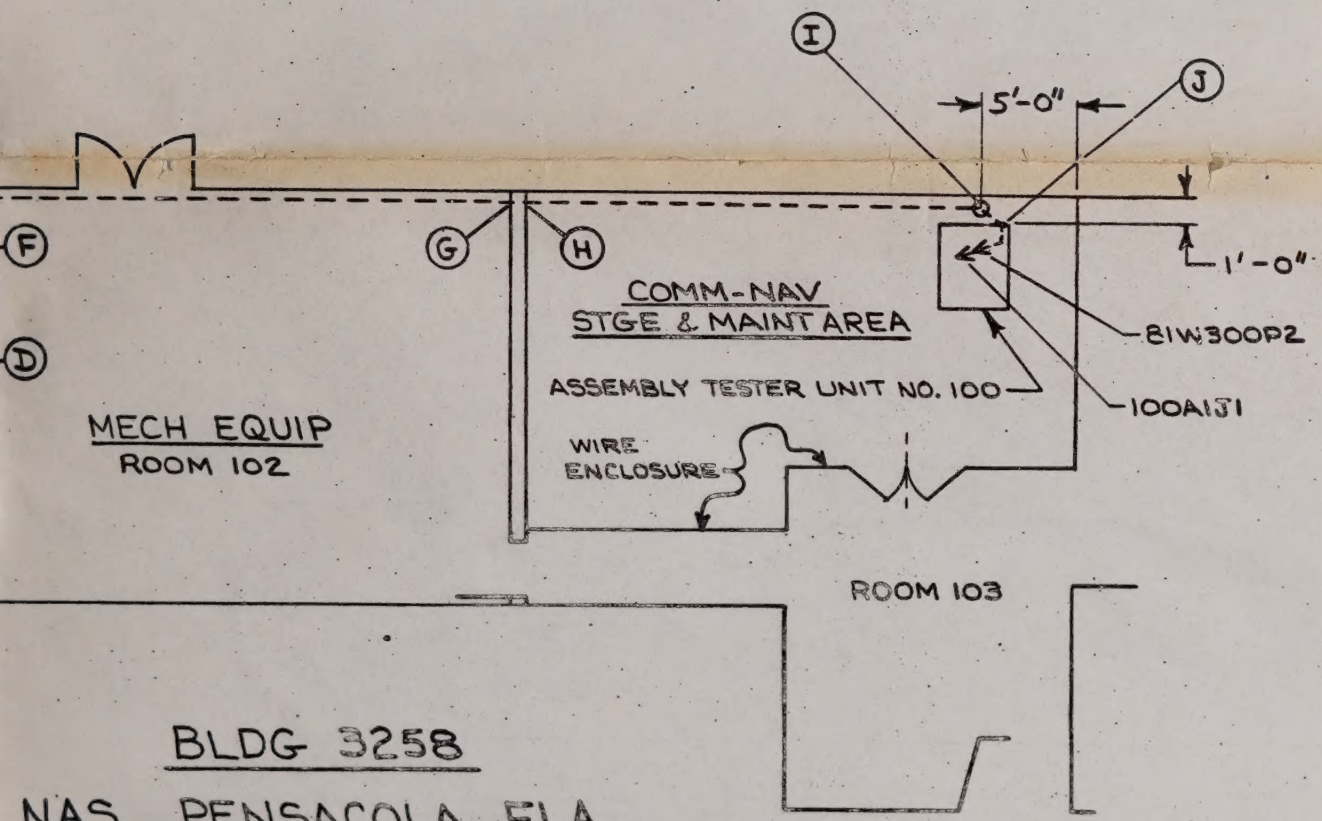
SIZE		REV
C	63C502198	

UTING, CABLE NO. 81W300

LE VERTICALLY DOWN WALL & ROUTE
FLOOR TO UNIT 100. ENTER UNIT
OMMET OPENING IN LEFT SIDE
OWER BACK CORNER, ROUTE
LLY TO BACK OF COMM PANEL
NATE AT 100A1J1

REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED



BLDG 3258

NAS, PENSACOLA, FLA

E

D

C

B

FOLD

REV

SIZE C 63C502198

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES—
TOLERANCES ON:
2-PLACE DECIMALS ±
3-PLACE DECIMALS ±
ANGLES ±
ALL SURFACES

MATERIAL—
GOVT OR COML
GE

SIGNATURES		DATE
DRAWN	R Cowan	6-8-72
CHECKED	R.C.	6-9-72
ISSUED	R Cowan III	6-9-72
ENGRG	E Jones	6-9-72
MFG		
MATLS		

GENERAL ELECTRIC
AGS DEPT LOC DAYTONA BEACH, FLA

TITLE
ROUTING DIAGRAM
81W300 SYSTEM SIGNAL CABLE
COMM-NAV TRAINER DEVICE 1D23

CONTRACT NO.

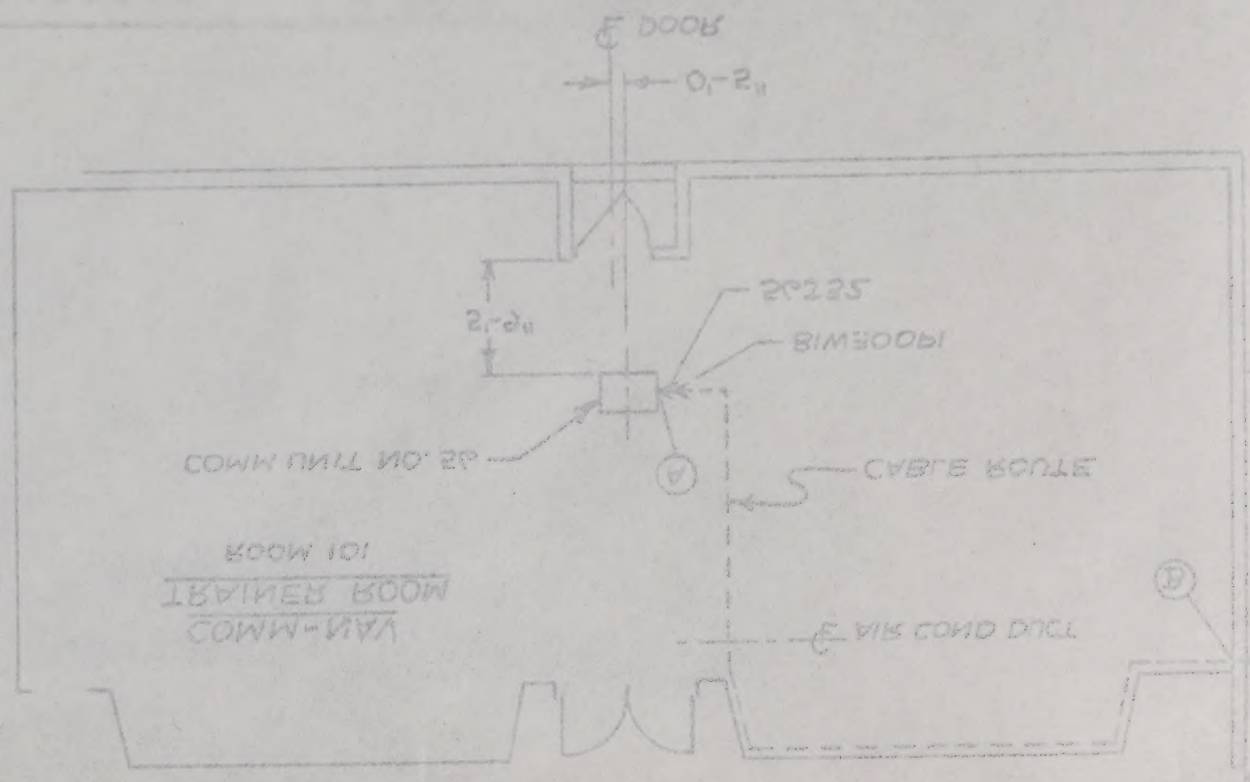
CODE IDENT. NO.	SIZE	DWG NO.
16331	C	63C502198

SCALE 1/100 | WT CALC ACTUAL | SHEET — CF —

PRINTS TO

FOLD

4 | 3 | 2 | 41A | 1



(I) (H) TO	WALL NEARS AND BEAM 2'-4" CEILING ROUTE CABLE HORIZONTALLY ON RM 104
(H) (G) TO	IN RM 104 BELOW 2'-4" CYPRUM PLASTER CEILING PENETRATE 8" CONCRETE BLOCK WALL
(G) (F) TO	ACROSS ROOM ROUTE CABLE HORIZONTALLY ON WALL
(F) (E) TO	CEILING LEVEL (2'-10" HIGH CEILING) CABLE RISES VERTICALLY ON WALL TO NEAR
(E) (D) TO	DUCT TO CORNER OF ROOM ROUTE CABLE HORIZONTALLY ON WALL BELOW
(D) (C) TO	AIR INTAKE DUCT APPROX 8 FT TO UNDERSIDE OF OUTSIDE CABLE RISES VERTICALLY ON RM 105 WALL
(C) (B) TO	BELOW ELEVATED FLOOR LEVEL PENETRATE 8" CONCRETE BLOCK WALL
(B) (A) TO	DUCT AT DUCT-CABLE INTERSECTION INDICATED ROUTE BELOW ELEV ELR & OVER TOP OF A/C
(A)	UNIT 2A CABLE BUCKET BELOW ELEV ELR LEVEL CABLE CONNECTOR 2C125 ON LEFT FACE OF
FROM PXM	CABLE ROUTING: CABLE NO. BIM3009

(1) TO (1)	8" TEE INTERM PANEL THRU ACROSS DROP C
FROM PXM	CABLE

ELECTRIC

DATE

SIGNATURE

UNLESS OTHERWISE SPECIFIED